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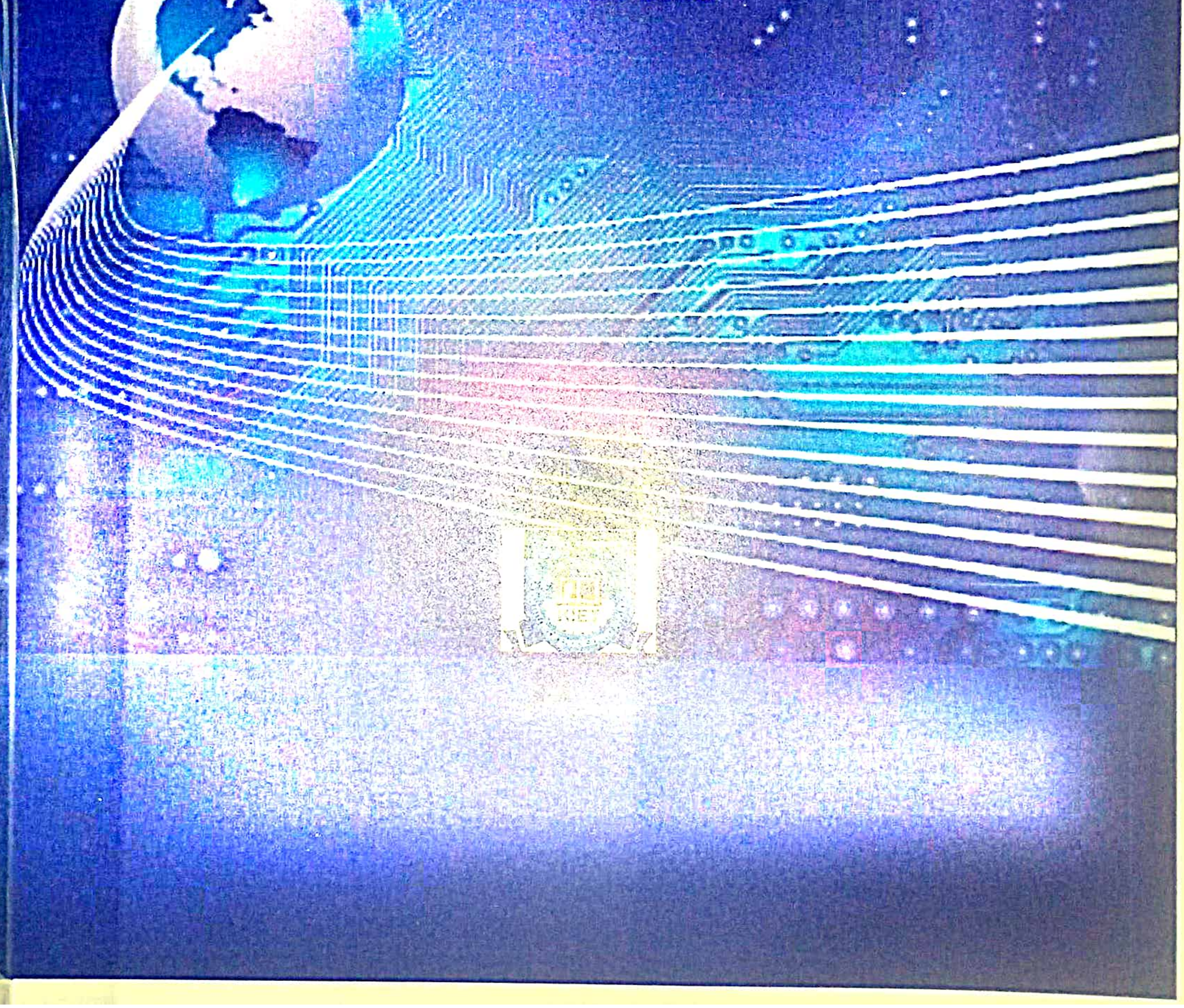

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Editorial

Wireless technology is very much in demand these days. There are different Directions of Arrival (DOA) techniques by which we can estimate the incoming signals the comparison between different Directions of Arrival techniques such as Sub Array beam forming based DOA, Capon & MUSIC (Multiple Signals Classification) DOA. Sub Array Beam forming based Direction of Arrival Estimation (SBDOA) technique is used & then comparison with other existing techniques.SBDOA technique gives the best results than other existing techniques.

A chirped short intense laser pulse in vacuum in external magnetic field studied as well as the variation of field & phase is studied.

Designing of combinational circuits using Inhibitor. Why INHIBITOR? Already we have NAND AND NOR Gate which are known universal gate. There is another universal gate "INHIBITOR". The purpose of using this gate is to reduce propagation delay.

Magnetic sensors are widely used in various applications such as consumer electronic products (mobile phones, laptops), biomedical applications (brain function mapping), navigation, vehicle detection, mineral prospecting, non contact switching (keyboard), contactless temperature measurement, wireless sensor network etc. Sensitivity of MagFET devices towards magnetic field, depends on the shape, dimensions VGS ,VDS. In this paper we have measured effect of Physical design of gate on sensitivity of MagFET.

A Dual band SIW Bowtie Antenna for X – Band applications is presented. The SIW technology has been used to design the antenna in a bow tie structure. The antenna has a dual band working at frequencies 10.19 GHz and 11.12 GHz. The simulated gains at these frequencies are 10 dB and 8.6 dB respectively. HFSS simulation software is used for all the simulations.

Solar energy is playing a pivotal role in compensating the electrical energy. As we all know that there is short fall in this energy due to more demand and decline trends of conventional source of energies and exhaustion of fuels like coal, petroleum, natural gases. To cope up with this trend of energy photovoltaic installation is being done in an electrical system to compensate and enhance the energy. Filtering data in real-time requires dedicated hardware to meet demanding time requirements. If the statistics of the signal are not known, then adaptive filtering algorithms can be implemented to estimate the signals statistics iteratively. Modern Field

A newly wired network was needed to get online. Even wired telephones are becoming a thing of past. Nowadays, Mobile networks have full-blown tremendously in the last four decades. The inception was the Cellular concept which was introduced with 1G, where, 'G' stands for generation networks. It had grown so fast, from generation to generation, nurturing from 1G, 2G, 3G, and finally, launched to 4G. And, today, we are using 4G technologies. And, also, 5G technology is almost ready to spread its wings to storm this competitive global mobile network market. Integrated Research on 5G is being carried on and is expected to come in usage commercially by 2020.

Preface

Dear Researchers,

We take this opportunity to welcome you all to the Volume No 6, Issue No. 1 of International Journal of Communications & Electronics (KIET - IJCE). This journal will provide a forum for in depth and substantial discussions on the theory, design and implementation of the emerging technologies in Communications, Networking, Microwave and Electronics techniques, thus providing solutions and strategies for business resilience.

It gives us an immense pleasure to have an amalgam of researchers from the fields of Communication Engineering, Electronics, and related technologies. The purpose of the Journal is to provide a platform to foster interdisciplinary communication among the delegates and to support the sharing process of diverse fields in various concepts and principles related to these domains.

Our appreciation also goes to entire team whose dedication and timeless efforts have gone for number of days for the second issue of the Journal.

Editors

Message

I am delighted to note that the Department of Electronics and Communication Engineering, KIET Group of Institutions, Ghaziabad is introducing Volume No 6, Issue No. 1 of International Journal of Communications and Electronics (KIET - IJCE).

I appreciate the efforts on the part of the Editorial Committee in bringing out an issue on Communications, Networking, Microwave and Electronics techniques.

I understand that the papers contributed for publication in the Volume No 6, Issue No. 1 are on almost all the current aspects of Communication Systems, Electronics systems, Microwave Engineering, Signal Processing & Applications, Networking Technologies and several others.

I have great pleasure in congratulating the Editors of this issue of KIET - IJCE for their untiring efforts in bringing out this sixth Volume No 6, Issue No. 1 of KIET-IJCE which will be a valued treasure for all who pursue research in Communications, Networking, Microwave and Electronics Engineering areas.

Let me close with warmest regards.

Dr. (Col) A Garg
Director
KIET

It is our pleasure that KIET is releasing the sixth volume of International Journal of Communications and Electronics (KIET - IJCE). Education is the base for building a good naon and we feel proud to be the contributor of such transformaonal naon.

I appreciate the efforts on the part of the Editorial Committee in bringing out an issue on Communications, Networking, Microwave and Electronics techniques.

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Dr Manoj Goel
Joint Director
KIET

Message

It gives me immense pleasure in writing this foreword for the Volume No 6, Issue No.1 of the KIET International Journal on Communications and Electronics (KIET - IJCE). This journal is targeted towards researchers, professionals, educators and students to share innovative ideas, issues, recent trends and future directions in the fields of Electronics and Communication Engineering.

The Volume No 6, Issue No. 1 of the journal KIET-IJCE includes papers on the theory, design and implementation of the emerging technologies in the field of Communications, Networking, Microwave and Electronics techniques. Furthermore, it will enable the researchers in various domains to foster the exchange of concept, protypes, research ideas and the results of research work which could contribute to the academic arena and also befit business and industrial community.

Dr. Sanjay Sharma
Editor – in - chief
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A Comparison of Sub Array Beam forming Technique with others Directions of Arrival Estimation Techniques

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Abstract: There are different Directions of Arrival (DOA) techniques by which we can estimate the incoming signals. In this research paper, I proposed the comparison between different Directions of Arrival techniques such as Sub Array beam forming based DOA, Capon & MUSIC (Multiple Signals Classification) DOA. Sub Array Beam forming based Direction of Arrival Estimation (SBDOA) technique is used & then comparison with other existing techniques. In this technique the antennaarray is decomposed in to two equal size virtual sub array. Two virtual sub arrays are used to form a signal whose phase relative to the reference signal & it is a function of the DOA.The DOA is then estimated based on the computation of the phase shift between the reference signal and its phase-shifted version. The phase-shifted reference signal is obtained after interference rejection through beam forming; the effect of interference on the process is significantly reduced by the use of this technique. SBDOA technique gives the best results than other existing techniques.

Index terms: **Beam forming, Direction of Arrival (DOA), Estimation, Uniform Linear Array (ULA), Pilot signal.**

INTRODUCTION

There are various techniques by which we can estimate the direction of arrival such as multiple signal classification (MUSIC) and estimation of signal parameters via rotational invariance technique (ESPRIT) and CAPON technique. I amdiscussingonlythree techniques as SBDOA (SubArray Beam forming based Direction Of Arrival), MUSIC and CAPON, further i will compare all the three techniques. In MUSIC-class techniques, the DOAs are determined by finding the directions for which their antenna response vectors lead to peaks in the MUSIC spectrum formed by the eigenvectors of the noise subspace,the capacity of DOA estimation using MUSIC is no more than M-1 where, M is the number of antenna elements in the antenna array [2]. In the capon technique we are using the minimum variance distortion less response algorithm to find out the estimated DOA, in the capon technique we are try to minimize the output power of the system except that the desired signal directions [3]. MUSIC DOA estimation gives more accurate result than capon method for two closely located signals, with small array element number; the capon method results give more error than MUSIC method results. Generally these techniques are not very effective to find out the better resolute estimated DOA. Further, using these techniques in the presence of multiple signal sources, the DOAs of the target signals and interference are all estimated, and as a consequence, these techniques cannot identify which signal source corresponds to which estimated DOA. To find out a better result in DOA estimation, a new sub array beam forming-based DOA (SBDOA) estimation technique that uses a reference signal (pilot signal) is used; the major difference between the used SBDOA estimation technique and existing techniques is that in the SBDOA estimation technique, the target DOA is estimated after interference rejection using Beam forming.

In other existing techniques, the DOA estimation is based on either computing the spatial signatures or antenna response vectors, as a result, a DOA is estimated in the presence of many other signals from sources other than the target one and, therefore, the performance of DOA estimation algorithms is significantly degraded by the interference.

In the used SBDOA estimation technique, the target DOA is estimated from the phase shift introduced in the actual signal by sub array beam forming, which is a function of the target DOA. Since the phase shift is estimated after sub array beam forming, all signals and interference other than the target one can be efficiently rejected or separated before DOA estimation. Thus their interference on the DOA estimation is reduced. In this way, the estimation resolution and accuracy of the used SBDOA technique are better than those of other existing techniques. The capacity of DOA estimation using SBDOA technique can be far larger than the number of antenna elements. The SBDOA technique is computationally simpler and can be easily implemented in terms of hardware. Further, the use of a reference signal that can be either a pilot signal or a decision - directed signal enables the used SBDOA technique to identify which signal source corresponds to which estimated DOA.

FORMATION OF SIGNAL MODEL

In the SBDOA technique we are using the uniform linear array (ULA) antenna geometry, the antenna array is decomposed into two equal-sized sub arrays such that for each element in one sub array, there is a corresponding **element** in the other sub array displaced by a fixed translational distance. Here we discuss the commonly used uniform linear array (ULA) and the SBDOA technique can be easily applied to other kinds of antenna arrays. Consider an M-element ULA with adjacent element spacing D deployed at a base station. Let angle θ_k in radians denote the DOA of the signal from source k. The M dimensional column vector $a(\theta_k)$, known as the antenna-array response vector is given by [1]

$$a(\theta_k) = [1 \; z(\theta_k) \ldots\ldots z(\theta_k)^{M-1}]^T$$

Where $z(\theta_k) = e^{-j2\pi D \sin\theta_k/\lambda}$ and λ is the wavelength

Figure 1 shows that general configuration for a ULA antenna having M elements arranged along a straight line with the distance between sensor elements, d, equal to one half of the incoming signal wavelength, λ. The angle of the incoming signal α is measured relative to the antenna bore sight. Here α angle can be taken as angle 0, it is just for the reference purpose.

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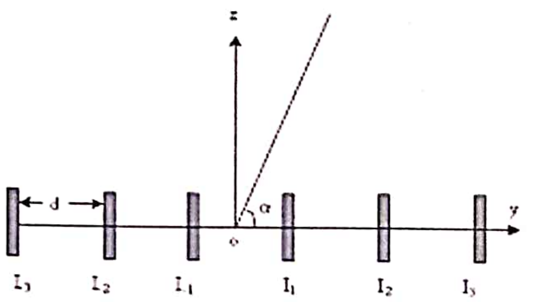

Fig1: Uniform Linear Array (ULA)

We assume that signals from different sources are uncorrelated or have negligible correlation with each other. If there are K signal sources and J unknown interference sources, then the received signal at the antenna array after down-converting to baseband can be represented by the M-dimensional vector as

$$u(t) = \sum_{k=1}^{K+J} s_k(t)a(\theta_k) + n(t)$$

Where $s_k(t)$ for k = 1, 2... K is a target signal component, $s_k(t)$ for k = K+1, 2...K+J is an unknown interference component, and $n(t)$ is a stationary background noise vector.

BEAM FORMING

Beam forming is signal processing technique that is used in sensor array to find out the directional signal transmission and reception. A Beam former is an array of sensors which can do spatial filtering, the objective is to estimate the signal arriving from the desired direction in the presence of noise and other interfering signals, a beam former does spatial filtering in the sense that it separates two signals with overlapping frequency content originating from different directions. Beam forming is the method used to create the radiation pattern of the antenna array by adding constructively the phases of the signals in the direction of the targets/mobiles desired, and nulling the pattern of the targets/mobiles that are undesired/interfering targets, this can be done with a simple FIR (Finite Impulse Response) filter. The weights of the FIR filter may also be changed adaptively, and used to provide optimal beam forming, in the sense that it reduces the MMSE between the desired and actual beam pattern formed.

SUB ARRAY BEAM FORMING BASED DIRECTION OF ARRIVAL ESTIMATION

The block diagram of the used SBDOA system is illustrated in Figure, two virtual sub arrays are used in conjunction with two sub array beam formers to obtain an optimum estimation of a phase-shifted reference signal whose phase relative to that of the reference signal is a function of the target DOA, the target DOA is then computed from the estimated phase shift between the phase-shifted reference signal and the reference signal [1]. Consider the case where θ_k for k = 1, 2,……,K is the target DOA to be estimated.

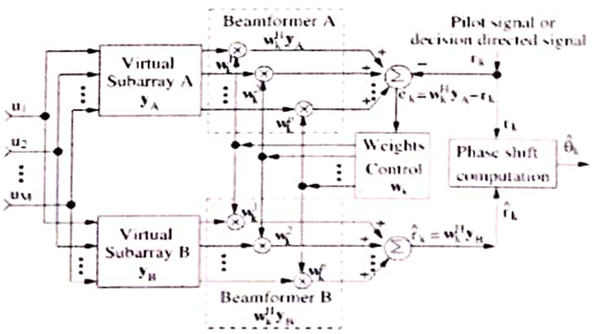

Fig2: Block Diagram of SBDOA

The function of the used DOA estimator is as follows. Two sub arrays signal vectors y_A and y_B are formed such that the phase shift between each signal component in y_A and its corresponding signal component from the same source in y_B is a function of the DOA, the two sub array signals are then fed into beam formers A and B. The weight vector w_k is obtained by minimizing the mean-square error (MSE) e_k between the output signal of beam former A and the reference signal r_k, using the weight vector w_k obtained from beam former A, the sub array signal y_B is weighted and combined in beam former B.

The output of beam former B, i.e., r_k is an optimum estimation of the phase-shifted reference signal and, further, the phase of r_k relative to that of the reference signal r_k is a function of the target DOA, θ_k, finally, the estimation $\hat\theta_k$ of the target θ_k is obtained based on the computation of the phase shift between the phase-shifted reference signal r_k and the reference signal r_k.

SUB ARRAY SIGNAL FORMATION

The ULA is deployed at the receiver, and two kinds of antenna element multiplexing geometries can be used to obtain two virtual sub arrays as:

(1) Maximum Overlapping Sub arrays (MOSs)

(2) Conjugate Sub arrays (CSs).

Consider an M-element ULA deployed at a receiver, MOSs have two sets of (M-1)-element virtual sub arrays, A and B. Sub array A consists of the first M-1 elements of the M-element antenna array deployed at the receiver and sub array B consists of the last M-1 elements. In CSs, each virtual sub array has the same number of elements as the antenna array deployed, Using the SBDOA technique, CSs lead to more efficient sub array beam forming and provide higher estimation accuracy and resolution of the DOA than MOSs

COMPUTATION OF DOA

Let $\hat{r}_k(t) = (w_k^B)^H y_B(t)$ denote the output signal of beam former B. Since $\hat{r}_k(t)$ is an optimum estimation of the phase shifted reference signal $e^{j\phi_k} r_k(t)$ in the MMSE (Minimum Mean Square Error) sense, it can be written as

$$\hat{r}_k(t) = e^{j\phi_k} r_k(t) + n_k(t)$$

This represents the reference signal shifted by ϕ_k plus an estimation error.

$\hat{r}_k = [r_k(1) r_k(2) \dots\dots r_k(L)]^T$

$r_k = [\hat{r}_k(1)\hat{r}_k(2) \dots\dots \hat{r}_k(L)]^T$

Let denote vectors with samples of the reference signal and the estimated phase-shifted reference signal in a snapshot interval, respectively, if $\hat\phi_k$ denotes an estimate of ϕ_k, it can be computed using the least square method such that the square error between the two signal vectors $\hat{r}_k$ and r_k is minimized, i.e.,

$$\underset{\hat\phi_k}{\text{minimize}} \left\| \hat{r}_k - e^{j\hat\phi_k} r_k \right\|$$

If, $e^{j\phi_k} = p + jq$ where, $p^2 + q^2 = 1$, the optimization problem in the above equation can be written as

$$\underset{p,q}{\text{minimize}} \ f(p,q) = \| \hat{r}_k - (p + jq) r_k \|$$

$$\text{subjected to} \quad p^2 + q^2 = 1$$

This optimization problem can be easily solved using the Lagrange multipliers method and the solution $\hat\phi_k$ can be obtained as

$$\hat\phi_k = \arg(p + jq) = \arg(r_k^H \hat{r}_k)$$

This is the angle of the complex inner product of the reference signal vector and its phase-shifted version, an estimation of the target DOA can then be obtained as

$$\hat\theta_k = \begin{cases} \arcsin\left(\frac{-\lambda\hat\phi_k}{2\pi D}\right), & \text{for MOSs} \\ \arcsin\left(\frac{\lambda\hat\phi_k}{2\pi D}\right), & \text{for CSs} \end{cases}$$

In the used technique, the DOA is estimated from the phase shift between the reference signal and its phase-shifted version, thus, the capacity of DOA estimation is no longer bounded by the number of antenna elements as in existing techniques Most importantly, the DOAs are estimated after interference rejection through sub array beam forming and, therefore, the effect of interference on DOA estimation is reduced.

SIMULATION RESULTS

In this section, the resolution, capacity, and accuracy of the SBDOA technique will be evaluated and compared with the other existing techniques through simulations. Here I am using Matlab tool to obtain simulation results.

The term resolution of DOA estimation is used to denote the minimum angle difference between two DOAs that can be resolved by the estimation technique. The term capacity is used to denote the maximum number of signal sources that a DOA estimation technique is capable of detecting. Firstly we compare the resolution of the SBDOA estimation using the MOS and CS and then after we will compare the resolution and capacity of the SBDOA estimation with the other existing techniques.

RESOLUTION OF SBDOA ESTIMATION FOR MOS & CS

This simulation result deals with a case where the DOAs of three signals and interference sources are closely distributed. A five-element ULA with a spacing of D = λ/2 deployed at the receiver was considered, three target signal components and one interference components with a pilot signal were assumed to be received at the antenna array with equal power. A snapshot length of 200 samples was used for both MOS and CS techniques. The vertical axis represents the occurrences as the number of times that a certain value of estimated DOA was obtained and the horizontal axis represents the estimated DOA in degree.

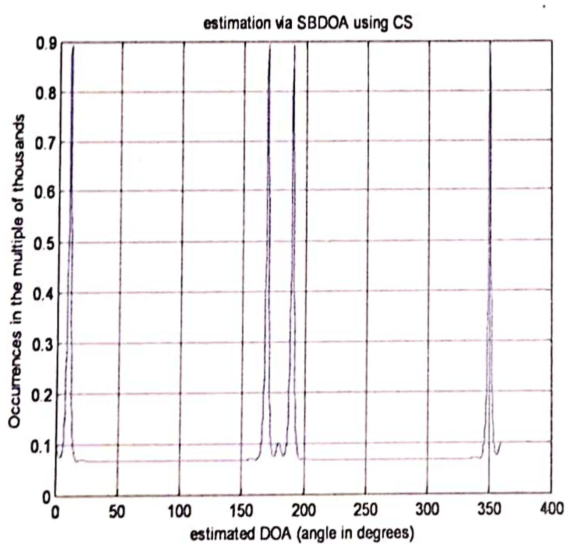

Fig3: Estimation via SBDOA using CSs.

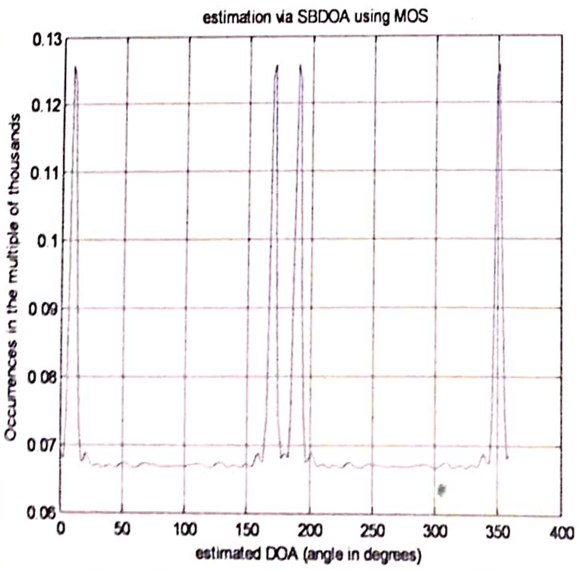

Fig4: Estimation via SBDOA using MOSs.

In this simulation result the actual DOA of the target signal is set at 170, 180 and 350 degree angles, and one interference is set at 10 degree angle, from the simulation results we can say that the resolution of the SBDOA technique using CSs is better than using MOSs, this is due to the fact that CSs have one more antenna element than MOSs in each sub array, which will lead to higher SINR (Signal to Interference plus Noise Ratio) at the beam former output for CSs Because MOSs contains only M-1 elements of the sub array then its SINR is less than the SINR of CSs, an increase in SINR leads to better estimation accuracy.

COMPARISON OF THE RESOLUTION & CAPACITY OF DOA ESTIMATION

In this simulation result we compare the resolution and capacity of the SBDOA technique with the other existing techniques like MUSIC and CAPON; here we are taking the Comparison of resolution and capacity of DOA estimation when the number of signal and interference sources is larger than the number of antenna elements, all the simulation conditions kept the same as in the previous section of simulations. Here we have simulation result of (1) SBDOA technique using CSs, (2) SBDOA technique using MOSs. (3) MUSIC, (4) Capon techniques.

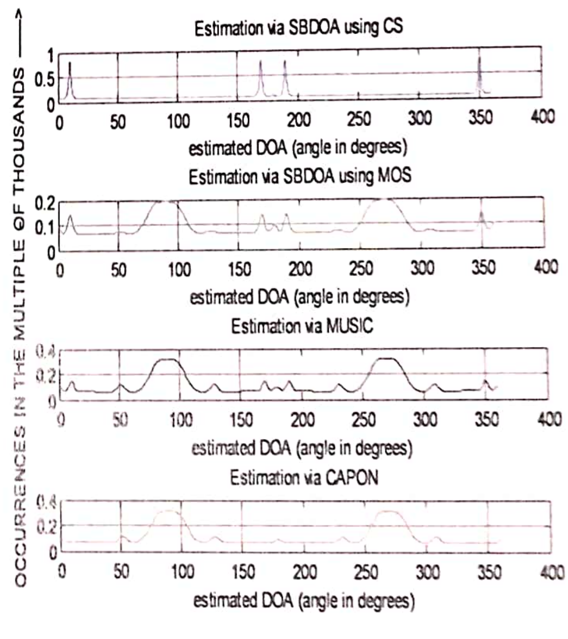

Fig5: Comparison between different DOA estimation techniques.

In this case of SBDOA using CSs we have the three target DOA at 170 , 180 and 350 degree angles, and one interference at 10 degree angle, in the SBDOA using MOSs we have also three target DOA at 170, 180 and 350 degree angle, and interference at 10, 90 and 270 degree angle, in the MUSIC technique we have three target signal at 170, 180 and 350 degree angle and it have more number of interference than SBDOA at 10, 50, 90, 130, 270 and 310 degree angle, the capon technique does not provides any target DOA and also it have more number of interference than SBDOA and MUSIC techniques. As shown from the simulation result the resolution of the three target DOA in SBDOA technique using CSs and MOSs is much better than the MUSIC and CAPON techniques, the MUSIC and CAPON technique having low SINR than SBDOA therefore these techniques have poor resolution In terms of capacity the SBDOA, and MUSIC estimation technique detecting three target signals but CAPON technique does not detecting any target signals

CONCLUSION

The comparison between different estimation technique has been proposed, in Sub Array Beam Forming-based Direction of Arrival

Estimation (SBDOA) technique, the two sub array beam formers are used to obtain an optimum estimation of the phase-shifted reference signal whose phase is relative to the reference signal and which is a function of the target DOA, the target DOA is estimated from the phase shift between the reference signal and its phase-shifted version, and the DOA is estimated after the interference rejection through beam forming in this way, the effect of interference on DOA estimation is reduced and the number of detectable signal sources can exceed in terms of the number of antenna elements, means detectable signal sources does not depends on the number of antenna elements used. Performance analysis and extensive simulations show that the used technique SBDOA offers significantly improved resolution, capacity, and accuracy of the estimation relative to the other existing techniques.

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The Study of a Chirped Short Intense Laser Pulse In Vacuum in External Magnetic Field and The Variation of Field & Phase

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ABSTRACTS

A chirped short intense laser pulse in vacuum in external magnetic field studied as well as the variation of field & phase is studied. During the study when we fixed some parameters like laser intensity parameter, pulse duration and spot size etc. it found that the energy gain increases on increasing the phase value. In this study we took the phase values viz. $\phi = \pi/2$, $\pi/3$, $\pi/4$ and $\pi/6$. The maximum value is found at $\phi = \pi/2$, and minimum is at $\phi = \pi/6$. Also the variation of energy gain and normalized magnetic field shows that the energy gain is higher when for larger value of laser spot size and energy gain attains higher value when b_0 lies between 0 to 5.

Keywords: Laser acceleration, chirped short intense laser pulse, phase and magnetic field.

INTRODUCTION

There are many techniques for chirping the pulse, the technique of chirped pulse amplification (CPA) which was invented around 1980's and has revolutionized laser technology [1] with its effect and uniqueness on that time. The experiments show that the chirp can be generated due to dispersion of materials they propagate through. There are some advantages of a vacuum as compared to medium over plasma for electron acceleration. Laser acceleration play important role in laser-plasma because the laser acceleration of particles are preferred since they are compact and having low-cost alternative to the conventional acceleration schemes [2]. The most cases reveals that the high intensity laser pulse initially propagate through an underdense plasma before reaching the critical density surface. Particle accelerators invented in 20th century and have found applications with a wide range of fields not only in our life but also in research & development and in our society etc. The longitudinal momentum increases when there is an increment in longitudinal force [3], also some authors found that the electron energy gain during acceleration by a linearly polarized chirped laser pulse is higher than that of the case of unchirped laser pulse. Interaction of electrons with strong fields is much attracting and the acceleration of electrons by a laser in a vacuum has been investigated theoretically [4-7]. A linear frequency chirp increases the time duration of laser-electron interaction and the magnetic wiggler is very useful in improving the strength of ponderomotive force $\mathbf{v}\times\mathbf{B}$, it deflects the electron periodically in order to keep it traversing in the accelerating phase up to longer distance [8]. When we apply a suitable frequency chirp in this case the energy of the electrons increases significantly and the quasimonoenergic collimated GeV electrons can be produced using a right choice of laser spot size, frequency chirp, and pulse duration [9]. It is noticed that the electrons are generated close to the rising edge of the laser pulse, trapped by the low intensity and never experience the peak of the pulse, and gain low energies. The electron can obtain net energy from a chirped electromagnetic plane wave in which the instantaneous frequency changes with the interaction time [10]. The parametric study of electron acceleration by a chirped Gaussian laser pulse was followed [11]. For the propagation distances much grater than the Rayleigh length, the modifications indicate that the temporal shape of the chirped laser beam will be changed and for propagation distances less than the Rayleigh length, the change in laser pulse shape is not considerable [12]. During last few years many views come out by the study for the tight focusing of the laser pulse for electron acceleration in vacuum [13-16]. Remarkable progress in development of high power femtosecond pulses and their applications has been achieved using chirped pulse amplification method [17-18]. The maximum electron energy gain during the acceleration by linearly polarized chirped laser pulse is higher than that of the case of unchirped laser pulse. Earlier study of vacuum electron acceleration schemes by using a chirped laser pulse, where the effect of a magnetic field was also considered and the laser field in our previous work was also linearly polarized [19-20]. The retained electron energy depends strongly on frequency chirp parameter and initial position of the electron [21]. We have more reviews on these extreme laser–matter interactions [22-23].

ELECTROMAGNETIC FIELDS AND ELECTRON DYNAMICS

The equations for the propagation of a laser pulse with electric field as given below

$$\mathbf{E} = \hat{x}\,E_x + \hat{z}\,E_z \tag{1}$$

The electric field component E_x and E_z can be written as

$$E_x = \frac{E_0}{f}\cos(\phi)\exp\left[-\frac{(t - z/c)^2}{\tau^2} - \frac{r^2}{r_0^2 f^2}\right] \tag{2}$$

$$E_z = -\frac{E_0}{f}\left[\frac{2x}{kr_0^2 f^2}\sin(\phi) + \frac{x}{z\left(1+(Z_R/z)^2\right)}\cos(\phi)\right]$$

(3)

Where

$$\phi = \omega(t)t - kz + \tan^{-1}(z/Z_R) - \frac{kr^2}{2z\left(1+\left(\frac{Z_R}{z}\right)^2\right)}$$

(4)

$\omega(t) = \omega_0(1-\alpha t)t$ and $f^2 = 1+\left(\frac{z}{Z_R}\right)^2$,

$k = \frac{\omega(t)}{c}$,

$Z_R = kr_0^2/2$ is the Rayleigh length,

$r^2 = x^2 + y^2$, r_0 is the minimum laser spot size,

and c is the velocity of light,

k is the laser wave number,

z_L is the initial position of the pulse peak,

τ is the pulse duration,

r is the radial coordinate,

ω_0 is the laser frequency at $z = 0$ and α is known as frequency chirp parameter.

The magnetic field related to the laser pulse is given by

$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$ where

$\mathbf{B}_L = \hat{y}B_y + \hat{z}B_z$. Now specifying the symbols

$$B_z = -\frac{E_0}{f}\left[\frac{2y}{kr_0^2 f^2}\sin(\phi) + \frac{y}{z\left(1+\frac{1}{\alpha^2}\right)}\cos(\phi)\right]\exp\left[-\frac{(t-z/c)^2}{\tau^2} - \frac{r^2}{r_0^2 f^2}\right]$$

(5)

Suppose an external axial magnetic field writing in vector form,

$\mathbf{B}_A = (-x\hat{y})\frac{B}{r_0}\exp\left(-\frac{x^2}{2r_0^2}\right)$ is applied along y-direction to the laser pulse then the resultant field can be written as

$$\mathbf{B} = \mathbf{B}_L + \mathbf{B}_A$$

(6)

The above equations governing electron momentum and energy has been solved by Runge-Kutta (RK4) method, we took into account initially the electron takes position at origin. Here e is the electronic charge having value 1.6 x 10^{-19} J and the value of rest mass of the electron (m_0) is 9.1 x 10^{-31} Kg. In this paper we introduced following dimensionless variables.

$a_0 \rightarrow \frac{eE_0}{m_0\omega c}$, $b_0 \rightarrow \frac{eB_0}{m_0\omega}$, $b_z \rightarrow \frac{eB_z}{m_0\omega_0 c}$,

$r_0 \rightarrow \omega_0 r_0/c$, $x \rightarrow \omega_0 x/c$, $z \rightarrow \omega_0 z/c$,

$z_L \rightarrow \omega_0 z_L/c$, $Z_R \rightarrow \omega_0 Z_R/c$, $t \rightarrow \omega_0 t$,

$\tau \rightarrow \omega_0\tau$ and $\alpha \rightarrow \alpha/\omega_0$.

RESULTS AND DISCUSSION

Figure 1 shows relativistic factor gamma γ as a function of z. Here we fixed some parameters for figure 1(a)-1(d), laser spot size r_0 = 100; pulse duration τ = 60, initial value of momentum p_{z0} = 0 and the chirp parameter (α) takes values α =1.0x10^{-5}, 1.5x10^{-5}, 2.0x10^{-5}; also the magnetic field b_0 =0.1, 0.2 and 0.3. Here the value of phase (ϕ) is different for figure 1(a)-1(d). For figure 1(a)-1(d) α =1.0x10^{-5}& b_0 =0.1 (shown by red dotted line), when α =1.5x10^{-5}& b_0 =0.2 (shown by green dotted line) and when α =2.0x10^{-5}& b_0 =0.3 (shown by blue dotted line). We observed that the chirp parameter (α) as well as phase plays important roll in energy enhancement. There are three value of chirping parameters and an external axial magnetic field ids applied. The electron experiences a force by the resultant field of the lasers and during acceleration it gains high energy. For a suitable chirped frequency the electron accelerates to high energy and here the amplitude of electron oscillations is small in comparison with wavelength. Therefore, the electron is in a spatially uniform chirped electric field. The laser frequency chirping plays important role to increase the transverse momentum of the electron. When the transverse momentum increases then longitudinal momentum also increases due to the longitudinal $\mathbf{v} \times \mathbf{B}$ force enhancement. The energy enhancement takes place on increasing the laser intensity and chirp parameters simultaneously. Figures 1(a)-1(d) show that the nature and the behaviour of curves are approximately same i.e. the smoothly changing curves show the energy variation is different for every curve. With chirp parameter the energy gain increases. The electron is accelerated within a few degrees to the axial direction. Here we observe that the energy gain going on increasing with phase. The maximum values of energy gain is when phase ϕ is $\pi/2$ and minimum for $\phi = \pi/6$. On increasing the phase the energy gain increases.

KIET IJCE KIET International Journal of Communications & Electronics
Volume. No. 6, Issue No. 1, Jan-June 2018, ISSN: 2320 – 8996

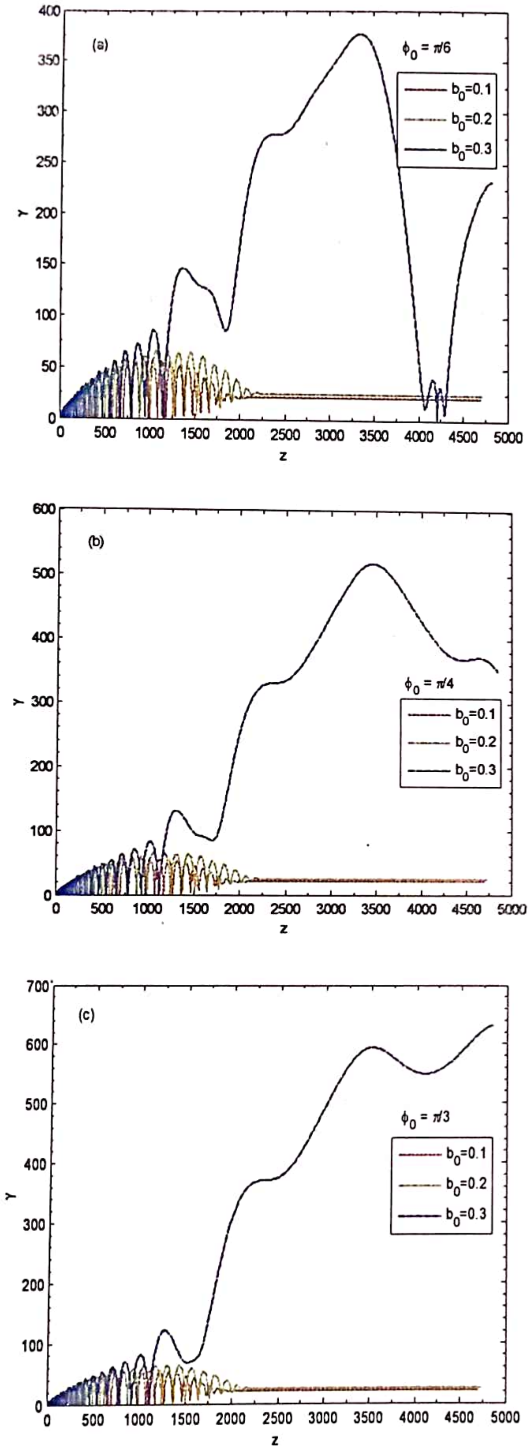
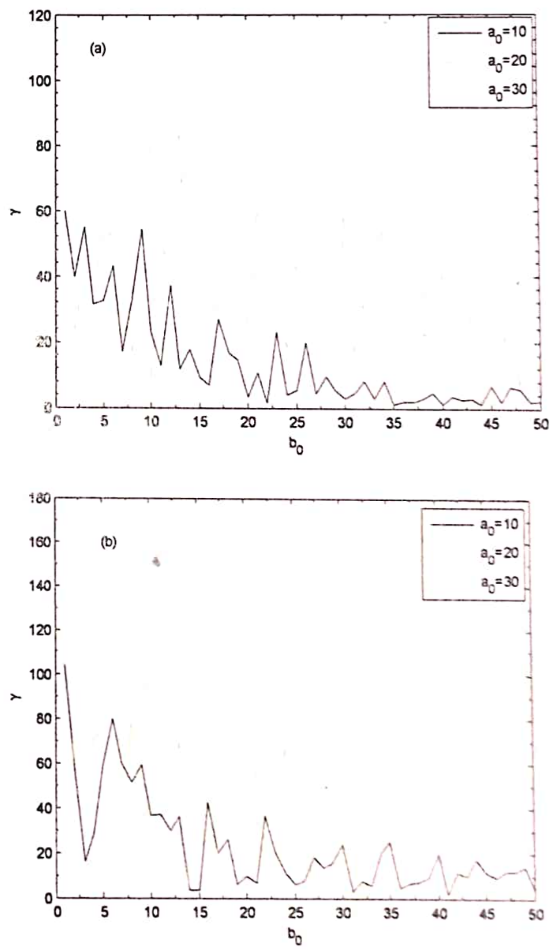


Figure 1 relativistic factor gamma γ as a function of z. Here α takes values α =1.0x10^{-5}, 1.5x10^{-5}, 2.0x10^{-5}; and b_0 =0.1, 0.2, 0.3. Also a_0 =10; r_0 =100; p_{z0} =0 and τ =50].

Figure 2 shows the relativistic factor gamma γ as a function of normalized magnetic field b_0. For figures 2(a)-2(b) we took some common parameters like, pulse duration τ =50; laser intensity parameter, a_0 =10, 15 and 20; Here the chirp parameter α =3.0x10^{-5}, 4.0x10^{-5} and 5.0x10^{-5}.The value of phase (ϕ) is π /3, π /4 and π /2 respectively corresponding to laser intensity parameter. But for figure 2(a) r_0 =75 and 100 for figure 2(b).

We don't consider the tight focussing effect of the beam when the beam waist size is large compared to laser wavelength. We know that the higher value of frequency chirp parameter reduces the electron energy gain during acceleration because the rate of frequency chirp of laser pulse decreases and reduces the rate of frequency chirp. In some situations a high electron energy can be achieved if the electron is injected with finite kinetic energy between ultra-high intensity chirped lasers. From these two figures we observe that the

energy gain is higher for figure 2(b) and this higher value is only when the normalized magnetic field lies between 0 and 5. The behaviour for both is same but not identical.



[Figure 2 the relativistic factor gamma γ as a function of normalized magnetic field b_0. (a) r_0 =75; and (b) r_0 =150.

Also a_0 =10, 20 and 30 with corresponding values of $\phi = \pi/4$, $\pi/3$ and $\pi/2$; τ =50; α =3.0x10^{-5}, 4.0x10^{-5} and 5.0x10^{-5}].

CONCLUSIONS

The study of a chirped short intense laser pulse in vacuum in external magnetic field shows the variation of energy gain with normalized distance as well as with normalized magnetic field. When we take some fixed values of laser intensity parameter, pulse duration and spot size etc. then the energy gain increases on increasing the phase value. Here we take only four values of the phase values i.e. $\phi = \pi/2$, $\pi/3$, $\pi/4$ and $\pi/6$. The behaviour and nature of the curves of figure 1 are near about same but energy gain is different. The maximum value of it is observed at $\phi = \pi/2$, and minimum is at $\phi = \pi/6$. For each curve magnetic field is different. Also the observation for variation of energy gain with normalized magnetic field reveals that the energy gain is higher when for larger value of laser spot size only when we took fixed values of other parameters, and energy gain attains higher value when b_0 lies between 0 to 5

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KIET IJCE KIET International Journal of Communications & Electronics
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Novel Method for Designing Combinational Circuits using LabVIEW

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Abstract—Designing of combinational circuits using Inhibitor. Why INHIBITOR? Already we have NAND AND NOR Gate which are known universal gate. There is another universal gate "INHIBITOR". The purpose of using this gate is to reduce propagation delay. All combinational circuits can be designed using inhibitor gate. Some examples are: Half Adder, Full adder, Encoder, Decoder, Mux, De-Mux , Half subtractor, Full subtractor Sequential circuits can also designed by inhibitor gate such as flip flop. And we have same result as reduced propagation delay. We are designing all circuits through LabVIEW software. This software provides an environment of virtual instruments. LabVIEW (Laboratory Virtual Instrument Engineering Workbench) is a graphical programing environment based on graphical programming language G. LabVIEW works on a data flow model in which information within a LabVIEW program, called a virtual instrument (VI), flows from data sources to data sinks connected by wires.

Keywords- Inhibitors, LabVIEW, Encoder, Decoder, Mux, De-Mux, Flip Flop.

INTRODUCTION

The "G" programming language, as implemented in the National Instruments product "LabVIEW", allows the user to describe a program with a dataflow representation. Our goal is to apply the techniques and concepts of the current dataflow research towards the adaptation of G as an embedded software development tool. LabVIEW is dominant in the instrumentation industry. As the instrumentation industry makes use of more embedded systems, it becomes practical to consider extending LabVIEW's and G's functionality to target embedded systems. Formally, G is a homogeneous, multidimensional, dynamic dataflow language. G uses "structured dataflow" semantics to specify high level concepts (e.g. loops, conditional control flow, etc.) instead of using low levelactors and feedback. We compare G to other models of computation, such as cyclostatic dataflow, dynamic dataflow, and process networks. In particular, we look for what we can learn from these models to apply to G. This survey is a launching point for discussing possible changes to G. In the future, we will discuss what extensions may be necessary for G to be more useful for representing some of these models of computation. We will also discuss semantic and syntactic restrictions to G that may be helpful when using G to describe a particular computational model.

GATES USING LOGIC INHIBITOR

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions low (0) and high (1) represented by different voltage levels. Inhibitor can be used to design all the combinational circuits as well as all the logic gates.

TYPES OF INHIBITOR

AND TYPE INHIBITOR GATE

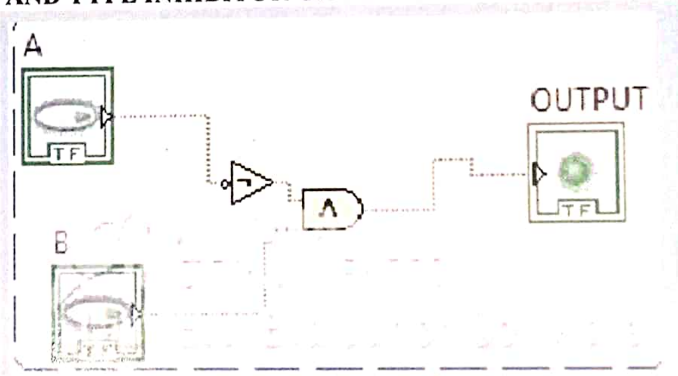


Fig 4.1 Block diagram of AND type inhibitor gate

OR TYPE INHIBITOR GATE

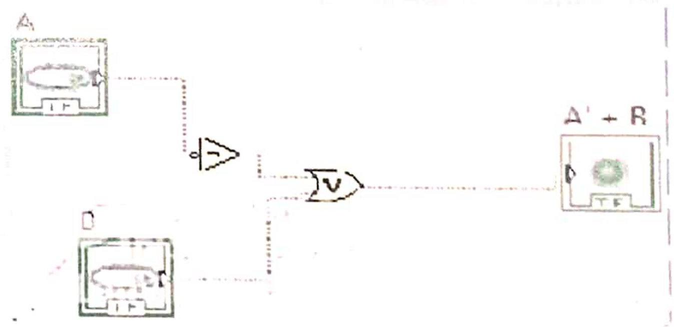


Fig 4.1 Block diagram of OR type inhibitor gate

DESIGNING OF LOGIC GATES
OR GATE

The *OR gate* gets its name from the fact that it behaves after the fashion of the logical inclusive "or." The output is "true" if either or both of the inputs are "true." If both inputs are "false," then the output is "false."

KIET IJCE KIET International Journal of Communications & Electronics
Volume. No. 6, Issue No. 1, Jan-June 2018, ISSN: 2320 – 8996

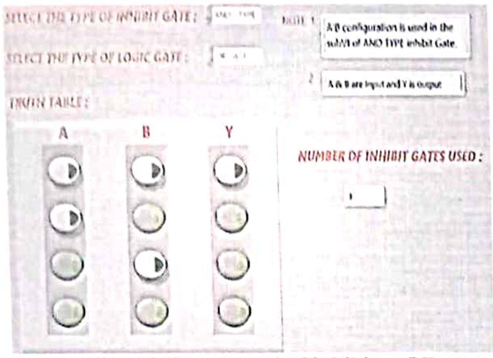


Fig. 4.3 Front panel of inhibitor OR gate

AND GATE

The AND gate is so named because, if 0 is called "false" and 1 is called "true," the gate acts in the same way as the logical "and" operator. The following illustration and table show the circuit symbol and logic combinations for an AND gate. (In the symbol, the input terminals are at left and the output terminal is at right.) The output is "true" when both inputs are "true." Otherwise, the output is "false."

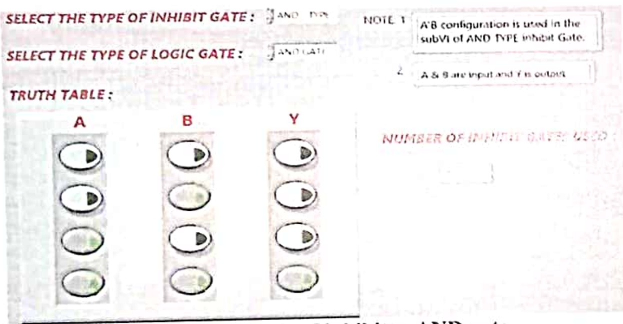


Fig. 2.4 Front panel of inhibitor AND gate

NOT GATE

A logical *inverter*, sometimes called a *NOT gate* to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state.

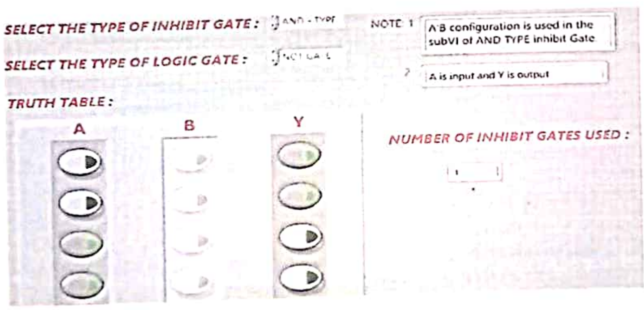


Fig. 2.5 Front Panel of inhibitor NOT gate

NAND GATE

The *NAND gate* operates as an AND gate followed by a NOT gate. It acts in the manner of the logical operation "and" followed by negation. The output is "false" if both inputs are "true." Otherwise, the output is "true."

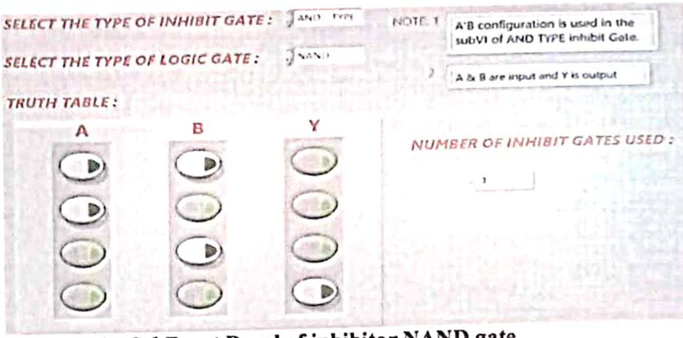


Fig. 2.6 Front Panel of inhibitor NAND gate

NOR GATE

The NOR *gate* is a combination OR gate followed by an inverter. Its output is "true" if both inputs are "false." Otherwise, the output is "false."

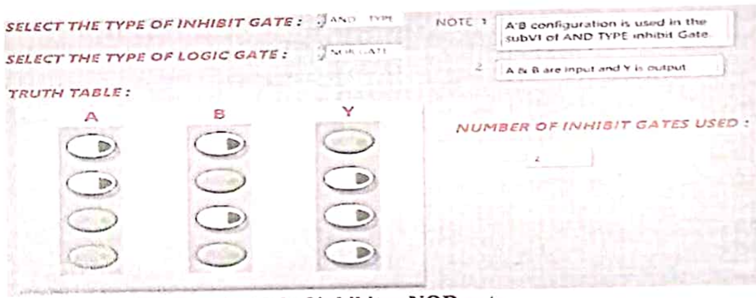


Fig. 2.7 Front Panel of inhibitor NOR gate

XNOR GATE

The XNOR (exclusive-NOR) gate is a combination XOR gate followed by an inverter. Its output is "true" if the inputs are the same, and "false" if the inputs are different.

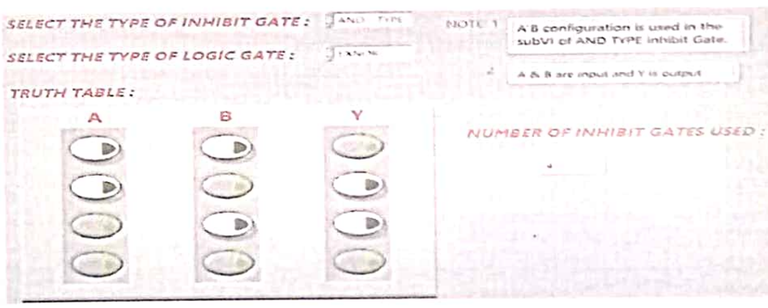


Fig. 2.8 Front Panel of inhibitor XNOR gate

XOR GATE

The XOR (exclusive-OR) gate acts in the same way as the logical "either/or." The output is "true" if either, but not both, of the inputs are "true." The output is "false" if both inputs are "false" or if both inputs are "true." Another way of looking at this circuit is to observe that the output is 1 if the inputs are different, but 0 if the inputs are the same.

KIET IJCE KIET International Journal of Communications & Electronics
Volume. No. 6, Issue No. 1, Jan-June 2018, ISSN: 2320 - 8996

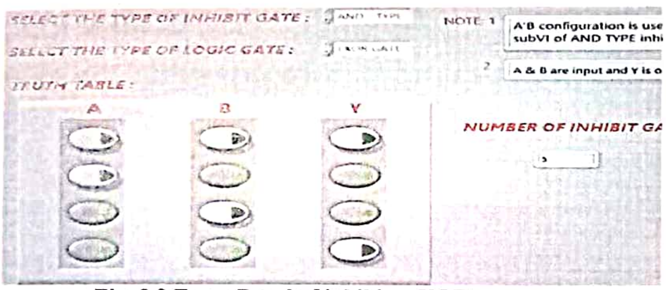


Fig. 2.9 Front Panel of inhibitor XOR gate

DESIGNING OF COMBINATIONAL CIRCUITS USING INHIBITOR GATE (AND TYPE)

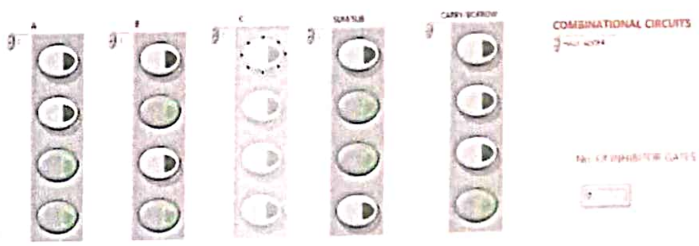


Fig. 3.1 Front Panel of inhibitor HALF ADDER

COMBINATIONAL CIRCUITS USING INHIBITOR

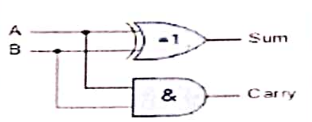
Combinational Logic Circuits are made up from basic logic NAND, NOR or NOT gates that are "combined" or connected together to produce more complicated switching circuits. These logic gates are the building blocks of combinational logic circuits. An example of a combinational circuit is a decoder, which converts the binary code data present at its input into a number of different output lines, one at a time producing an equivalent decimal code at its output.

Combinational logic circuits can be very simple or very complicated and any combinational circuit can be implemented with only NAND and NOR gates as these are classed as "universal" gates.

A Half Adder Circuit

A half adder is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits.Half Adder Truth Table with Carry-Out

Symbol:



Truth Table:

B	A	SUM	CAR
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the truth table of the half adder we can see that the SUM (S) output is the result of the Exclusive-OR gate and the Carry-out (Cout) is the result of the AND gate. Then the Boolean expression for a half adder is as follows.

For the **SUM** bit:

SUM = A XOR B = A ⊕ B

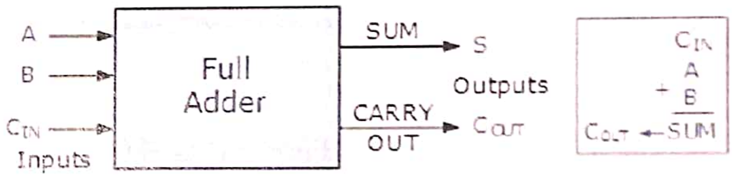
For the **CARRY** bit:

CARRY = A AND B = A.B

FULL ADDER

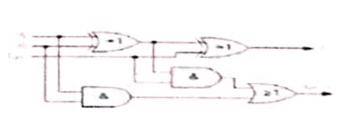
The main difference between the **Full Adder** and the previous **Half Adder** is that a full adder has three inputs. The same two single bit data inputs A and B as before plus an additional *Carry-in* (C-in) input to receive the carry from a previous stage as shown below.

Full Adder Block Diagram



Full Adder Truth Table with Carry

Symbol:



Truth Table:

C-in	B	A	Sum	C-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Then the Boolean expression for a full adder is as follows.

For the **SUM** (S) bit:

SUM = (A XOR B) XOR Cin = (A ⊕ B) ⊕ Cin

For the **CARRY-OUT** (Cout) bit:

CARRY-OUT = A AND B OR Cin (A XOR B) = A.B + Cin (A ⊕ B)

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Volume. No. 6, Issue No. 1, Jan-June 2018, ISSN: 2320 – 8996

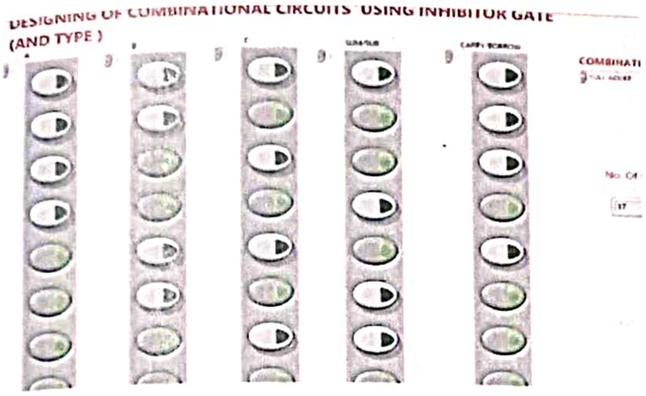
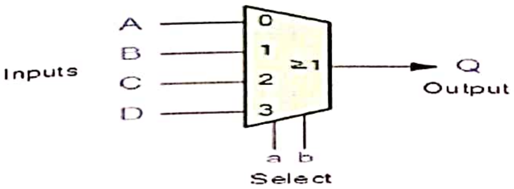


Fig. 3.2 (a) Front Panel of inhibitor FULL ADDER gate

MUX

The multiplexer is a combinational logic circuit designed to switch one of several input lines to a single common output line by the application of a control logic



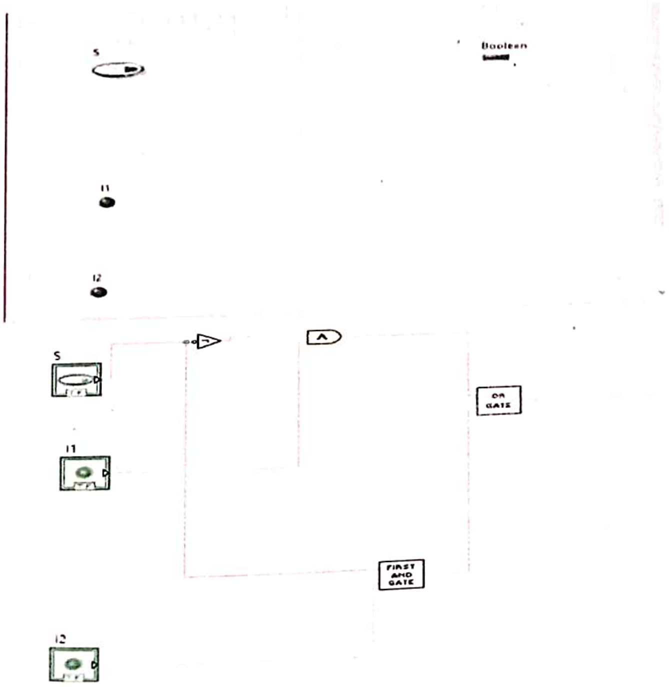
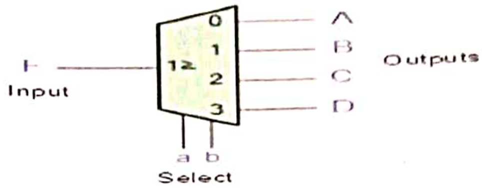


Fig. 3.2 Front Panel of inhibitor MUX Fig. 5.3 Block Diagram of inhibitor MUX gate

DEMUX

The demultiplexer is a combinational logic circuit designed to switch one common input line to one of several output line by the application of a control signal



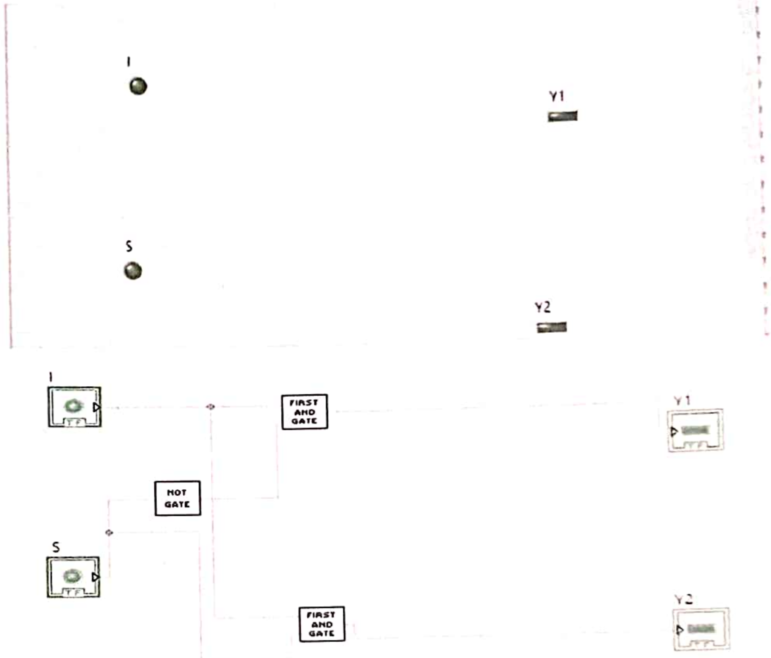


Fig. 3.4 Front Panel of inhibitor DEMUXFig. 3.5 Block Diagram of inhibitor DEMUX

ENCODER

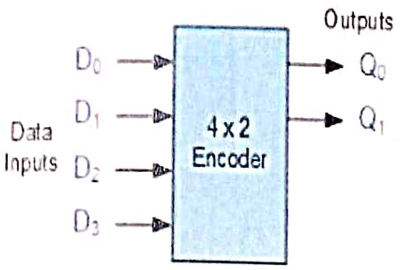
Unlike a multiplexer that selects one individual data input line and then sends that data to a single output line or switch, **Digital Encoder** more commonly called a **Binary Encoder** takes ALL its data inputs one at a time and then converts them into a single encoded output. So we can say that a binary encoder, is a multi-input

combinational logic circuit that converts the logic level "1" data at its inputs into an equivalent binary code at its output.

Generally, digital encoders produce outputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines. An "n-bit" binary encoder has 2^n input lines and n-bit output lines with common types that include 4-to-2, 8-to-3 and 16-to-4 line configurations.

to-2 Bit Binary Encoder

KIET IJCE KIET International Journal of Communications & Electronics
Volume. No. 6, Issue No. 1, Jan-June 2018, ISSN: 2320 – 8996



Inputs			
D_3	D_2	D_1	D_0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	0	0	0

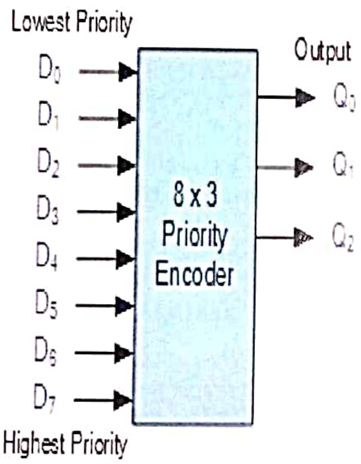
Fig. 3.6 Front Panel of inhibitor PRIORITY DECODERFig. 3.7 Block Diagram of inhibitor PRIORITY ENCODER

Priority Encoder

The **Priority Encoder** solves the problems mentioned above by allocating a priority level to each input. The *priority encoders* output corresponds to the currently active input which has the highest priority. So when an input with a higher priority is present, all other inputs with a lower priority will be ignored.

The priority encoder comes in many different forms with an example of an 8-input priority encoder along with its truth table shown below.

8-to-3 Bit Priority Encoder



Inputs							
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	X
0	0	0	0	0	1	X	X
0	0	0	0	1	X	X	X
0	0	0	1	X	X	X	X
0	0	1	X	X	X	X	X
0	1	X	X	X	X	X	X
1	X	X	X	X	X	X	X

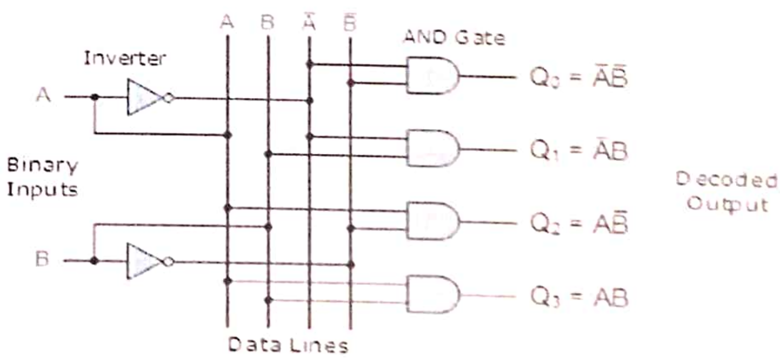
X = don't care

3.7 DECODER

The name "Decoder" means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output.

Binary Decoders are another type of digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an *n*-bit code, and therefore it will be possible to represent 2^n possible values. Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its *n* outputs to logic "1".

A 2-to-4 Binary Decoders.



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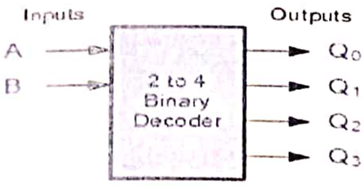
Volume. No. 6, Issue No. 1, Jan-June 2018, ISSN: 2320 – 8996



Truth Table

A	B	Q0	Q1
0	0	1	0
0	1	0	1
1	0	0	0
1	1	0	0

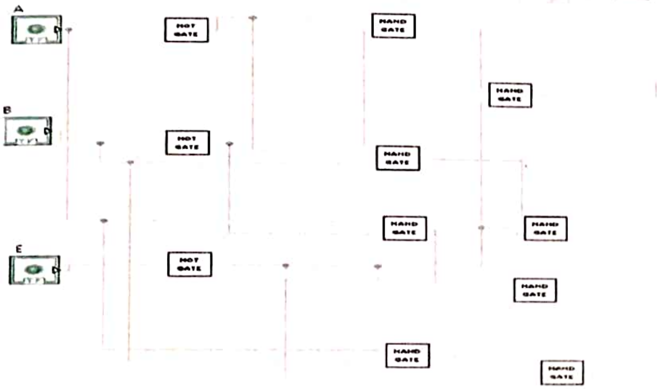


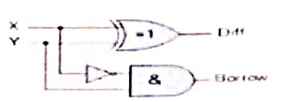
Fig. 3.8 Front Panel of inhibitor DECODER

Fig. 3.9 Block Diagram of inhibitor DECODER

HALF SUBTRACTOR

A half subtractor is a logical circuit that performs a subtraction operation on two binary digits. The half subtractor produces a sum and a borrow bit for the next stage.

Half Subtractor with Borrow-out

Symbol	Truth Table			
	Y	X	DIFFERENCE	BORR
	0	0	0	0
	0	1	1	0
	1	0	1	1
	1	1	0	0

From the truth table of the half subtractor we can see that the DIFFERENCE (D) output is the result of the Exclusive-OR gate and the Borrow-out (Bout) is the result of the NOT-AND combination. Then the Boolean expression for a half subtractor is as follows.

For the **DIFFERENCE** bit:

D = X XOR Y = X ⊕ Y

For the **BORROW** bit

B = not-X AND Y = X.Y

DESIGNING OF COMBINATIONAL CIRCUITS USING INHIBITOR GATE (AND TYPE)

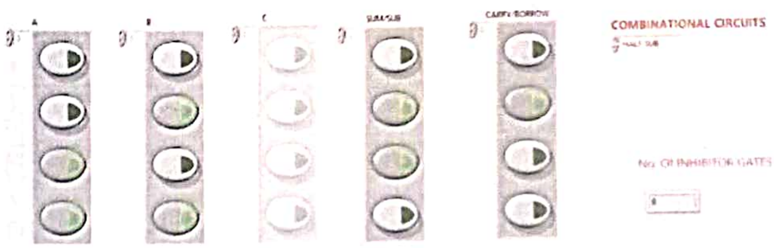


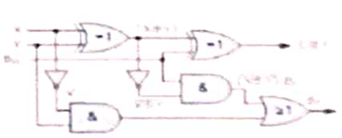
Fig. 3.10 Front Panel of inhibitor HALF SUBTRACTOR

FULL SUBTRACTOR

The main difference between the **Full Subtractor** and the previous **Half Subtractor** circuit is that a full subtractor has three inputs. The two single bit data inputs X (minuend) and Y (subtrahend) the same as before plus an additional *Borrow-in* (B-in) input to receive the borrow generated by the subtraction process from a previous stage as shown below.

Full Subtractor Block Diagram

Full Subtractor Truth Table

Symbol	Truth Table				
	B-in	Y	X	Diff	B-out
	0	0	0	0	0
	0	0	1	1	0
	0	1	0	1	1
	0	1	1	0	0
	1	0	0	1	1
	1	0	1	0	0
	1	1	0	0	1
	1	1	1	1	1

Then the Boolean expression for a full subtractor is as follows.

For the **DIFFERENCE** (D) bit:

KIET IJCE KIET International Journal of Communications & Electronics
Volume. No. 6, Issue No. 1, Jan-June 2018, ISSN: 2320 – 8996

$D = (X.Y.B_{IN}) + (X.Y.B_{IN}) + (X.Y.B_{IN}) + (X.Y.B_{IN})$

which can be simplified too:

$D = (X \text{ XOR } Y) \text{ XOR } B_{IN} = (X \oplus Y) \oplus B_{IN}$

For the **BORROW OUT** (B_{OUT}) bit:

$B_{OUT} = (X.Y.B_{IN}) + (X.Y.B_{IN}) + (X.Y.B_{IN}) + (X.Y.B_{IN})$

which will also simplify too:

$B_{OUT} = X \text{ AND } Y \text{ OR } (X \text{ XOR } Y)\, B_{IN} = X.Y + (X \oplus Y)\, B_{IN}$

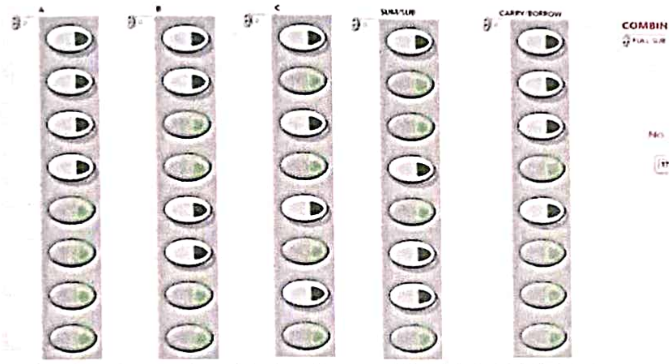


Fig. 3.11 Front Panel of inhibitor FULL SUBTRACTON

4. COMPARISON CHART BETWEEN SIMPLE LOGIC CIRCUITS AND LOGIC CIRCUITS USING INHBITOR ON THE BASIS OF PROPAGATION DELAY

S.NO.	LOGIC GATES	INHIBITOR LOGICGATES
1 AND GATE	1.483	1.48
2 OR GATE	1.473	1.457
3 NOT GATE	1.32	1.316
4NAND GATE	2.234	2.23
5 NOR GATE	2.29	2.28
6 XOR GATE	3.0741	3.075
7 XNOR GATE	3.245	3.236

The propagation delay using inhibitor is slightly greater than the other two universal gates (NAND and NOR).

FUTURE ASPECTS

Inhibitor is a universal gate but the propagation delay using inhibitor is more so further modifications are going on so that the propagation delay would be reduced and so that inhibitor can be used in many places.

CONCLUSION

Inhibitor is a universal logic gate. With the help of inhibitor we can design all the logic gates as well as all the combinational circuits.

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Design and analysis of MOS based Magnetic Field Sensor

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ABSTRACT

Magnetic sensors are widely used in various applications such as consumer electronic products (mobile phones, laptops), biomedical applications (brain function mapping), navigation, vehicle detection, mineral prospecting , non contact switching (keyboard), contactless temperature measurement, wireless sensor network etc . Sensitivity of MagFET devices towards magnetic field, depends on the shape, dimensions VGS ,VDS. In this paper we have measured effect of Physical design of gate on sensitivity of MagFET.

Keywords—Hall Effect, Magnetic sensor, MagFET device, CMOS Technology, Lorentz force

INTRODUCTION

Magnetic Field Effect transistor (MagFET) is unipolar transistor having one source & splitted drain. It is fully compatible with electronics devices because they share same substrate. There are many devices such as slider & flap mobile phone, laptops in which we have to measure magnetic field intensity to do desire work. When Magnetic Field is absent then it works normally as MOSFET but when we apply external orthogonal magnetic field then due to Lorentz force some part of current is deviated from one drain to another. We measure this current deviation and get sensitivity towards magnetic field. The advantage of the MagFET is it can be replace as electric to magnetic sensing element and vice versa.

WORKING PRINCIPLE OF MAGFET

When orthogonal magnetic field is applied to the channel, the carriers are deflected due to Lorentz's force. The split-drain MAGFET transistor senses the magnetic field and converts it into a corresponding electrical signal. When electric charge q moving with speed V in presence of external magnetic field B then charges deflected from their direction by the Lorentz force F.[5]

$F = q.E_H + q. (V\times B)$

V is average drift velocity of electron along the direction of drain.

$V = \mu n. E_E$

µn is drift mobility of electron in channel and EE is lateral electric field parallel to channel (due to drain voltage) & Current density Jn is defined as.

$Jn = n.q. \mu n.E_E$

The magnetic part of Lorenz force pushes electron towards one drain to another drain and creates some electron concentration gradient due to this phenomena Hall electric field (E_H) is appears between edges of drain. Force due to E_H is responsible for charge decrement at edges of drain and equilibrium is established.

$F = q. E_H + q. (V\times B) = 0$

$E_H = - (V\times B)$

$E_H = - \mu Hn (E_E\times B)$

µHn is Hall mobility for electron and it is different from drift mobility.

$\mu Hn = rH. \mu_n$

Here rH is Hall scattering factor. Its value depends upon thermal motion of electron. Drain current deviation (ΔI) is related to Hall electric field.

$E_H = - rH (Jn \times B) /n.q$

We conclude that Hall electric field is linear function of electron mobility, lateral electric field, and external magnetic field but inversely to carrier concentration.

The sensitivity of sensor depends on several factors e.g. the channel length and width, drain gap, source and drain contact sizes and the biasing conditions (V_{GS} and V_{DS}) and can be expressed by following equation. The quantity of current deviation (ΔI) is calculated by relative sensitivity of MagFET.

$\Delta I = B \cdot S \cdot I_D$

Where I_D is the bias current of MagFET, S is the relative sensitivity of MagFET, and B is the perpendicular magnetic field. If we increase the length of channel, Lorentz force will acting for longer time and we get appreciable amount of current deviation. Although we require long channel it will give smaller bandwidth, lesser chip density & increase noise level of device.

DESIGN METHOD

MagFET is very susceptible to its geometry. There are mainly three parameter which effect sensitivity significantly drain gap length, drain gap width, and aspect ratio. We havemeasured two types of gate design concave & convex. Concave MagFET drain gap region does not covered with SiO_2& polysilicon region but in convex MagFET is covered. We used rectangular copper wire to produce external orthogonal magnetic field.

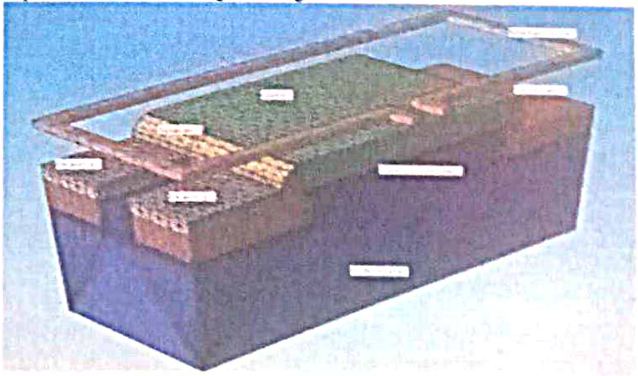

Fig. 2 Geometrical Design of MagFET

In Fig.2 MagFET comprises SiO_2& Si_3N_4 material which is used as gate oxide and spacer respectively. Source length is 40μm, width is 75μm and doping depth is 20μm. Drain1 and Drain2 have same dimension. Both have length 40μm, width 30μm and doping depth is 20μm. We have chosen drain gap length 10μm, 20μm, 30μm, 40μm & drain gap width 5μm, 10μm, 15μm. Channel design and concentration profile of MagFET shown in Fig 1 is listed in TABLE-I.

TABLE I
DEVICE DESIGN PARAMETERS

S.No.	Parameter	Value [unit]
1.	Gate Length	100 [μm]
2.	Channel Length	90 [μm]
3.	Channel width	75 [μm]
4.	Gate oxide thickness	2 [μm]
5.	Spacer thickness	10 [μm] each side
6.	Drain gap width	15 [μm]
7.	Drain gap length	30 [μm]
8.	Gate overlap	5 [μm] each side
9.	Substrate Doping	1×10^{17} [cm^{-2}]
10.	S/D Doping	5×10^{19} [cm^{-2}]
11.	S/D Extension Region	5×10^{18} [cm^{-2}]

When we apply magnetic field of 1T then due to Lorentz force current in drain2 (I_{d2}) is increased & simultaneously current in drain1 (I_{d1}) decrease. We get current difference $\Delta I = I_{d2} - I_{d1}$. When voltage V_{GS} is 1V and V_{DS} 1V then got current I_{d1} 4.52μA and current I_{d2} 1.46μA & sensitivity $0.33T^{-1}$.

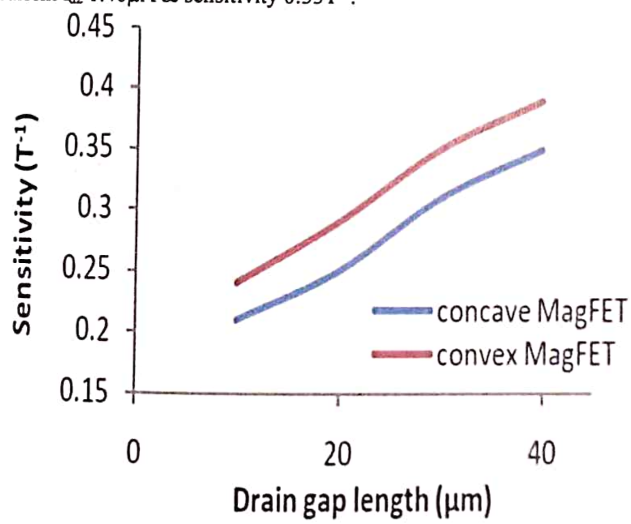

Fig 3. Variation in Sensitivity with Drain gap length

Fig 3 gives sensitivity of MagFET with variation of drain gate length when we fixed drain gap width at 10 μm.

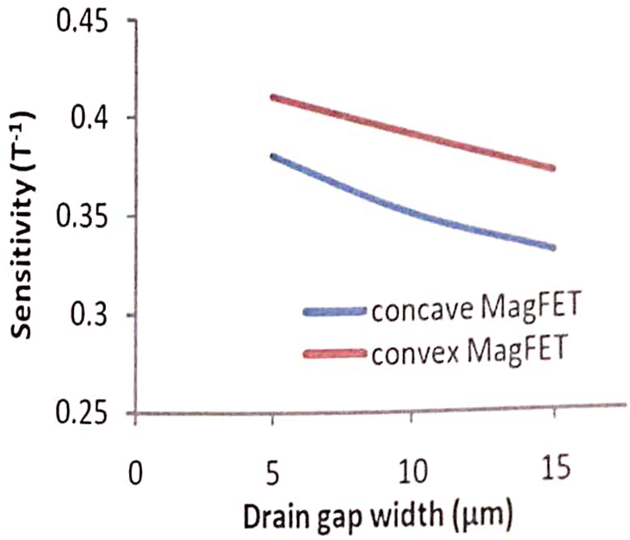

Fig 4. Variation in Sensitivity with Drain gap width (u)

CONCLUSIONS

We saw sensitivity of Convex MagFET is greater than concave MagFET. If we look for design issue then drain gap width should minimum because we are giving more space for charge deviation and drain gap length maximum because we provide maximum time & length for current deviation.

Convex MagFET is preferred at those places where we have to achieve higher sensitivity but its performance inhibits from linearity. If we don't want to avoid linearity property then we have to use Concave MagFET. In industry where linearity is major issue Concave MagFET is best option.

ACKNOWLEDGEMENTS

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Dual Band SIW Bowtie Antenna for X – band Applications

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ABSTRACT

A Dual band SIW Bowtie Antenna for X – Band applications is presented in this paper. The SIW technology has been used to design the antenna in a bow tie structure. The antenna has a dual band working at frequencies 10.19 GHz and 11.12 GHz. The simulated gains at these frequencies are 10 dB and 8.6 dB respectively. HFSS simulation software is used for all the simulations.

Keywords: Substrate integrated waveguide, Bow Tie Antenna, X band.

INTRODUCTION

The fundamental concept of Substrate Integrated Circuits (SIC) is to synthesize non planar structures in a planar form which is completely compatible with other planar structures. This can be achieved by creating artificial channels [1,4,7].

Substrate integrated waveguide is used as converting non planar structure to planar structure. It is a technology which is dielectric filled waveguide with metallic vias on the side walls of the waveguide. These artificial wave guiding channels are embedded in planar substrate with arrays of periodic metalized vias or slots.

The vias or slots act as electrical walls for waveguides. In [2] substrate integrated waveguide cavity backed slot antenna is used. Here bow tie antenna slot is cut to achieve broader bandwidth performance. A high gain bow tie antenna using substrate integrated technology has been presented in [3].

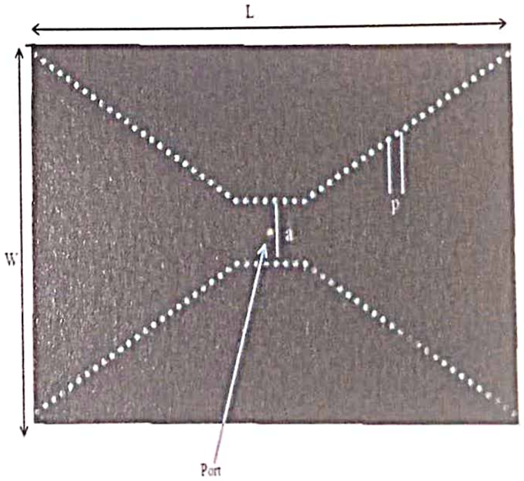
The antenna has a pair of bow tie radiator on the opposite of the common dielectric substrate. The bow-tie-shaped slot antenna is also studied as a most preferable antenna for broadband application since few years [3]. Studies on this type of antenna reported that this type of antenna has a potential to exhibit 20%–36% bandwidth with appropriate design of feeding network.

In this paper, a Dual band Bowtie antenna is designed using Substrate Integrated Waveguide (SIW). A SIW consists of substrate with metalized vias acting as two side walls and two metallic walls (upper and lower).

This antenna will work on a X – band frequency range (8-12 GHz). It is a low cost efficient design of a dual band antenna and will find a number of applications in the X-band frequency range. The basic parameters of antenna i.e. Gain, Radiation pattern, Current distribution and S – parameter are simulated in Ansys HFSS software [12].

ANTENNA DESIGN

The proposed configuration of bow tie substrate integrated waveguide is shown in fig 1. Bow tie antenna is formed by placing metallic vias in bow tie form. A bow-tie substrate integrated waveguide antenna is formed on a 0.8-mm-thick dielectric substrate with ϵ_r=2.33 (RT Duroid 5870). The metallic side walls of the antenna are used to avoid leakage. The feed of this antenna is excited by applying discrete port as shown in fig.1. Firstly SIW (substrate integrated waveguide) aims to work for a cut off frequency of 10 GHz with the design specifications of substrate integrated waveguide such as width of the SIW a= 8.30 mm, center-to-center distance between the metallic vias p= 2 mm and diameter of the metallic vias d= 0.8 mm. These values are calculated by using the design equations of SIW, given below:



antenna designed with design parameters L= 98mm, W= 60mm,ϵ_r= 2.33, h
Fig.1. Proposed geometry of SIW Bow =0.8mm, a= 8.30mm, p = 2 mm , R= 0.5

Deign Equations of Substrate Integrated Waveguide

SIW consists of two parallel conducting arrays of via holes represented by 'd'. *TE*10 mode is the dominant mode for wave propagation in SIW as of the conventional rectangular waveguide [5]. 'a' is the parameter between the two arrays which determines the propagation constant of the fundamental mode. Similarly parameters'd' is the diameter of vias d and p are set so as to minimize the leakage through the vias.

A. The metalized via hole diameter is

$d < \frac{\lambda_g}{5}$

B. The spacing between the via holes is

$P \leq 2d$

C. The physical width of SIW is

$w_{eff} = a - 1.08\frac{d^2}{p} + 0.1\frac{d^2}{a}$,where weff is the width of the waveguide.

Now this Substrate integrated waveguide is modified to form the antenna in Bow tie type (as shown in fig.1.). The bow tie substrate integrated waveguide is designed on RT duroid substrate with 0.8mm thickness. The substrate length 'L' of the antenna is 98mm and 'W'= 60mm. It is designed for the X- band Applications. The SIW is designed with the lowest dielectric constant (εr=2.33), distance between the consecutive cylinders, P =2mm. and the diameter of vias is 1mm. The aperture length is 60mm, flare angle is 26.56̊ and the distance between two parallel rows of vias is 10mm. Bow tie substrate integrated antenna has a dual band behavior working in two frequencies. The frequencies of the antenna are 10.19 GHz and 11.12 GHz. The above antenna has an application in X band.

RESULTS AND DISCUSSION

Return Loss

The designed antenna was simulated using software Ansys HFSS. The antenna is excited by using discrete port indicated in fig. 1. The simulated reflection coefficients of the antenna are shown given in Fig. 2. The operating frequencies of the antenna have an application in X band. The antenna has dual band characteristics with resonant frequency of 10.19 GHz and 11.12 GHz. The simulated return loss is value defined by S11 < −10 dB in 10.19 GHz is -27 dB and at 11.2 GHz is -24dB (as shown in fig.2.).

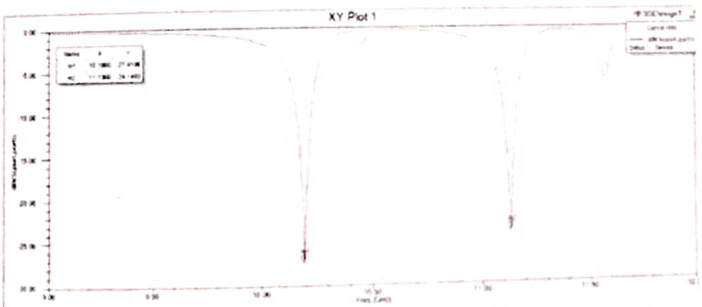


Fig.2 Return loss of the proposed antenna in dB showing two cutoff frequencies (Dual Band) at 11.12 GHz and 10.19 GHz

Current Distribution

The current distribution for the antenna is shown in fig.3 and fig .4. The current distribution is calculated for both of the frequencies of the antenna i.e. 10.19 GHz and 11.12 GHz.

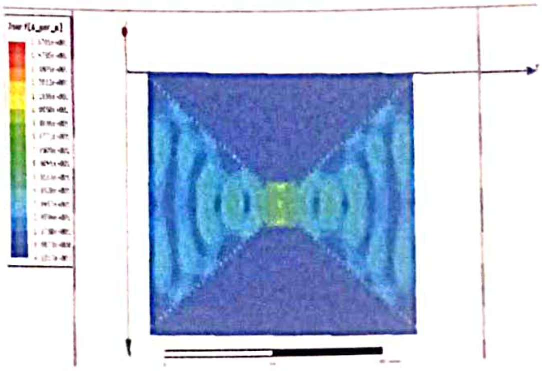


Fig. 3 Current Distribution in SIW Bowtie antenna at 10.19 GHz frequency

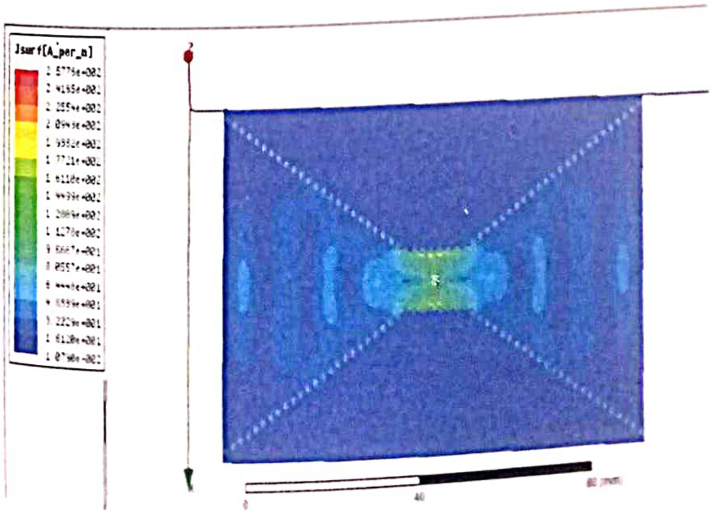


Fig. 4 Current Distribution in SIW Bowtie antenna at 11.12 GHz frequency

Radiation Pattern

The radiation pattern for the bow tie substrate integrated antenna is shown in fig.5. The antenna is radiated in both of the direction with a high gain at both the frequencies. The pattern demonstrated for the antenna is in end fire direction with a gain of 10 dB at 10.19 GHz and 8.6 dB at 11.12 GHz. Gain vs frequency plot is calculated (as shown in fig. 6) for different frequencies.

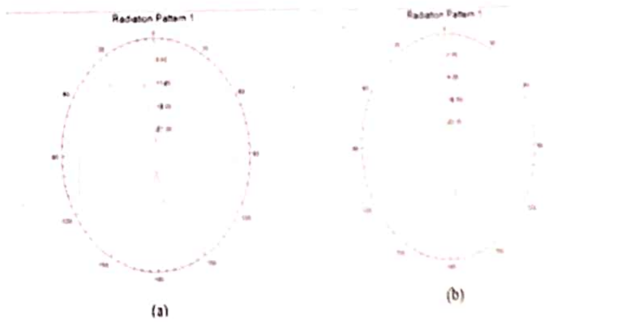


Fig. 5. Radiation Pattern of the bow tie substrate integrated waveguide at (a) 10.19 GHz and (b) 11.12 GHz

Fig. 6 Gain vs frequency plot for the proposed antenn.

CONCLUSION

In this, a Dual band Bowtie antenna is designed using Substrate Integrated Waveguide (SIW). A SIW consists of substrate with metalized vias acting as two side walls and two metallic walls (upper and lower). This antenna will work on a X – band frequency range (8-12 GHz). It is a low cost efficient design of a dual band antenna and will find a number of applications in the X-band frequency range. This type of antenna shows a dual band behavior at two different frequencies i.e. 10.19 GHz and 11.12 GHz. The results are simulated using software Ansys HFSS.

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Maintenance Indication of Solar Panel and Theft Prevention

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ABSTRACT

Solar energy is playing a pivotal role in compensating the electrical energy. As we all know that there is short fall in this energy due to more demand and decline trends of conventional source of energies and exhaustion of fuels like coal, petroleum, natural gases. To cope up with this trend of energy photovoltaic installation is being done in an electrical system to compensate and enhance the energy. An photovoltaic installation in an electrical system made from the assembly of various photovoltaic units that uses solar energy to produce the electricity in a cheaper way from sun power. Till now the use and scope of solar energy is limited and has not reached up to masses. Moreover the efficiency of the system is also low due to which the output is not sufficient as compared to input, as in some installed case of solar panel it has been observed that efficiency is not more that 27%. To make it versatile and more useful for the masses newer trends and innovations will help.

Keywords: Photovoltaic, efficiency, solar energy.

INTRODUCTION

It is important and urgent to find alternative source to replace conventional fuel or to reduce its continuous consumption due to their limited reservoirs and bad impact on environment. So we have to find alternative source of energy. The proposed work performs the function are maintenance indication of solar panel using sensor and theft prevention. The efficiency of solar panel reduces due to dust deposited on the solar panel. To overcome this problem, a sensor is placed to alert for maintenance, based on Android Application developed for both maintenance and theft prevention. For maximum power extraction from the sun, a photovoltaic cell with MPPT (Maximum power point Tracking) system is used. This will increase the system efficiency.

METHOD AND IMPLEMENTATION

Parts of proposed system

The main blocks of this project are:

- Micro controller (Arduino)
- Reset button
- Crystal oscillator
- Regulated power supply (RPS)
- LED indicator
- Solar panel
- MOSFET

Description of components

Arduino

Arduino is a tool for making computers that can sense and control more of the physical world than your desktop Computer. It's an open-source physical computing platform based on a simple microcontroller board, and a Development environment for writing software for the board. Arduino can be used to develop interactive objects, taking inputs from a variety of switches or sensors, and controlling a variety of lights, motors, and other physical outputs. Arduino projects can be stand-alone, or they can communicate with software running on your computer (e.g. Flash, Processing.)

Regulated power supply (RPS)

The DC power supply is practically converted to each and every stage in an electronic system. Thus a common requirement for all these phases will be the DC power supply. All low power system can be run with a battery. But, for a long time operating devices, batteries could prove to be costly and complicated. The best method used is in the form of an unregulated power supply –a combination of a transformer, rectifier and a filter.

Solar panel

Solar Cells can be electrically connected together exactly the same way as batteries. Currents add when connected in parallel and stay the same when connected in series, while voltages add when connected in series and stay the same when connected in parallel. Modules of cells can be added together in the same fashion.

Individual solar cells are connected together in series to form a solar panel. The P side of one cell is connected to the N side of the next cell, and so on. As mentioned above, voltages add together to form higher voltages. Current stays the same for the whole panel as for one single cell.

Individual solar panels are connected in parallel to form a solar array. The voltage stays the same for the whole array as for the individual panels. The currents from the individual panels add together to form higher currents.

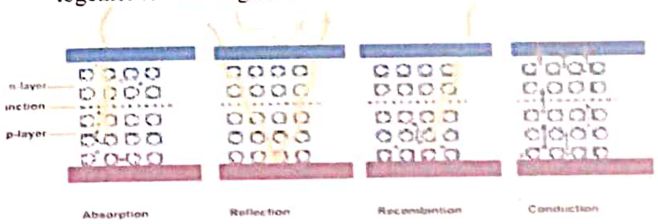

Figure 1 – Operation of a solar cell

Software Description
This project is implemented using following softwares:

- Express PCB – for designing circuit
- Arduino compiler - for compilation part
- Proteus 7 (Embedded C) – for simulation part

IMPLEMENTATION

1) Theft Prevention: To achieve this we use the GPS and GPRS features with accelerometer. If the Panel moves or unauthorized activity occurs then there is change in axis value of accelerometer which will be detected. It will process the data and notify the GPS location of Panel for tracking on web server as well as on mobile app. Alert action is defined on web server like email alert or sms.

2) Maintenance Indication: To achieve this function we use Dust, Voltage and Current Sensors. So when the deposition of dust on Panel increases the efficiency start to reduce, this can be monitored using the sensor values. It will update this data on webserver which can be viewed to know the time for maintenance of Panel.

CONCLUSION

The project "THE PREVENTION AND MAINTENANCE INDICATION OF SOLAR PANEL" where Consumers can easily monitor the battery voltage and solar panel voltage. According to the referral voltage action is taken by microcontroller.Use of microcontroller based systems provides huge computational capability and reduction in the hardware. Microcontroller is a mini computer and brings much more accuracy in the control of MOSFET and IGBT. The MPPT charge controller operates with high efficiency (90% or even higher) as compared to existing charge controllers.

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FPGA Implementation of Adaptive Filter

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Abstract

Filtering data in real-time requires dedicated hardware to meet demanding time requirements. If the statistics of the signal are not known, then adaptive filtering algorithms can be implemented to estimate the signals statistics iteratively. Modern Field Programmable Gate Arrays (FPGAs) include the resources needed to design efficient filtering structures. Furthermore, some manufacturers now include complete microprocessors within the FPGA fabric. This mix of hardware and embedded software on a single chip is ideal for fast filter structures with arithmetic intensive adaptive algorithms.
This paper aims to combine efficient filter structures with optimized code to create a system-on-chip (SoC) solution for various adaptive filtering problems. Several different adaptive algorithms have been coded in VHDL as well as in C for the Power PC 405-microprocessor. The designs are evaluated in terms of design time, filter throughput, hardware resources and power consumption.

Key Word: -Filters, Adaptive filters, Algorithm, FPGA, Arrays-Programming and System-on-chip.

INTRODUCTION

On systems that perform real-time processing of data, performance is often limited by the processing capability of the system. Therefore, evaluation of different architectures to determine the most efficient architecture is an important task. This topic discusses the purpose of the paper, and presents an overview and the direction.
The purpose of this paper is to explore the use of embedded System-on-Chip (SoC) solutions that modern Field Programmable Gate Arrays (FPGAs) offer. Specifically, it will investigate their use in efficiently implementing adaptive filtering applications. Different architectures for the filter will be compared. In addition, the Power PC embedded microprocessor will be employed for the various training algorithms. This will be compared to training algorithms implemented in the FPGA fabric only, to determine the optimal system architecture.
Digital Signal Processing (DSP) has revolutionized the manner in which we manipulate data. The DSP approach clearly has many advantages over traditional methods, and furthermore, the devices used are inherently reconfigurable, leading to many possibilities.
Modern computational power has given us the ability to process tremendous amounts of data in real-time. DSP is found in a wide variety of applications, such as: filtering, speech recognition, image enhancement, data compression, neural networks; as well as functions that are unpractical for analog implementation, such as linear-phase filters. Signals from the real world are naturally analog in form, and therefore must first be discretely sampled for a digital computer to understand and manipulate. The signals are discretely sampled and quantized, and the data is represented in binary format so that the noise margin is overcome. This makes DSP algorithms insensitive to thermal noise. Further, DSP algorithms are predictable and repeatable to the exact bits given the same inputs. This has the advantage of easy simulation and short design time. Additionally, if a prototype is shown to function correctly, then subsequent devices will also.
There are many advantages to hardware that can be reconfigured with different programming files. Dedicated hardware can provide the highest processing performance, but

is inflexible for changes. Reconfigurable hardware devices offer both the flexibility of computer software, and the ability to construct custom high performance computing circuits. The hardware can swap out configurations based on the task at hand, effectively multiplying the amount of physical hardware available. In space applications, it may be necessary to install new functionality into a system, which may have been unforeseen. For example, satellite applications need to be able to adjust to changing operation requirements. With a reconfigurable chip, functionality that was not predicted at the outset can be uploaded to the satellite when needed.

2 Programmable Logic Devices

Programmable logic is loosely defined as a device with configurable logic and flip-flops linked together with programmable interconnects. The first programmable device was the programmable array logic (PAL) developed by Monolithic Memories Inc. (MMI) in 1975. Considering that any Boolean function can be realized as a sum-of-products or equivalently as a product-of-sums by utilizing De Morgan's law, the PAL structure is rather intuitive. It generally consists of inputs with inverters leading into a series of AND gates whose outputs lead into a series of OR gates. This makes the products of any combination of the inputs and their complements available to the OR gates for the sum. A similar device, the programmable logic array (PLA), reverses the order of the AND and OR gates, which led to greater functionality. The reason is that the product terms can be shared across the OR gates at the outputs, effectively giving the chip more logic width. The structure in Figure 1 is a usual PLA before programming, with all possible connections are pre-wired typically by fuses. To implement a custom design, a programmer is used to blow the fuses with high current and break the unwanted connections.

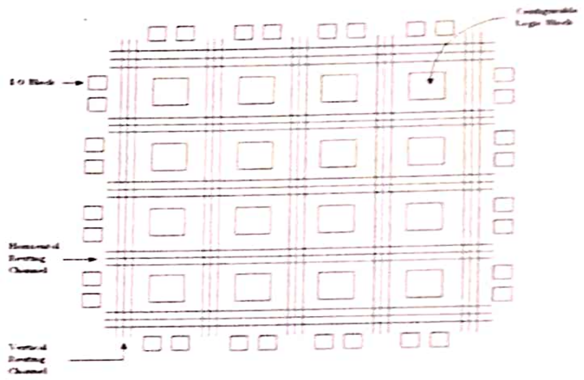

Fig. 1 PLA Structure

An improvement from PAL and PLAs came with the introduction of the complex programmable logic device (CPLD), which allows for more complex logic circuits. A CPLD consists of multiple PAL-like blocks connected by programmable interconnects. While PALs are programmed with a programmer, a CPLD is programmed in-system with the manufacturers' proprietary method or with a JTAG cable connected to a computer. CPLDs are well suited to complex, high-performance state machines. An alternative type of PLD developed more recently is the field programmable gate array (FPGA). Xilinx introduced the FPGA in 1984. These devices have a more flexible, gate-array-like structure with a hierarchical interconnect arrangement. The fundamental part of the FPGA is the look-up table (LUT), which acts as a function generator, or can alternatively be configured as ROM or RAM. They also include fast carry logic to adjacent cells making them suitable for arithmetic functions and further DSP applications.

3 FPGA Architecture

The majorities of FPGAs are SRAM-based and can therefore be programmed as easily as standard SRAM. The SRAM bits are coupled to configuration points in the FPGA (Figure 2 left) and controls whether or not a connection is made. This is normally accomplished by a passgate structure (Figure 2 right) that turns the connection on or off depending on the logic value (True or False) supplied by the SRAM. Because they are SRAM based, FPGAs are volatile. As such, they must be programmed each time power is applied. This is normally accomplished with another part of the circuit that reloads the configuration bit stream, such as a PROMThe configuration bit stream stored in the SRAM controls the connections made and also the data to be stored in the Look-up tables (LUTs). The LUTs areessentially small memories that can compute arbitrary logic functions. Each manufacturer has a distinct name for their basic block, but the fundamental unit is the LUT. Altera call theirs a Logic Element (LE) while Xilinx's FPGAs have configurable logic blocks (CLBs) organized in an array. The configurable logic blocks of an FPGA are generally placed in an island style arrangement. Each logic block in the array is connected to routing resources controlled by a interconnect switch matrix.

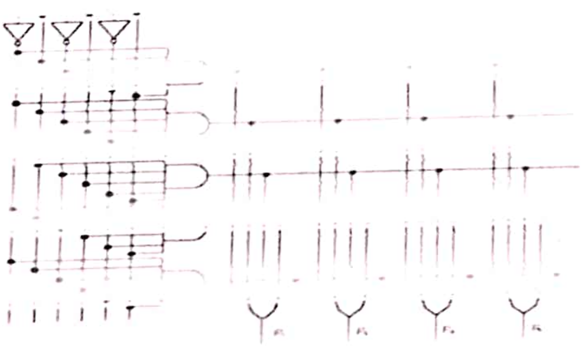

Fig. 3 FPGA cell Structure

With this layout, a very large range of connections can be made between resources. A downside to this flexible routing structure is that unlike the CPLD, signal paths are not fixed beforehand, which can lead to unpredictable timing. However, the tradeoff is the FPGA's increased logic complexity and flexibility. Each CLB in a Xilinx FPGA encompasses four logic slices, which in turn contain two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. The LUT is capable of implementing any arbitrary defined Boolean function of four inputs and the propagation delay is therefore constant regardless of the function. Each slice also contains flip-flops and a fast carry chain. The dedicated fast carry logic allows the FPGA to realize very fast arithmetic circuits.

Manually defining the routing connections in a programmable device may have been feasible with the early PALs but is nearly impossible considering the density of modern FPGAs. Configuring these programmable devices can be achieved in several ways, such as schematic design entry, the use of hardware description languages (HDLs), and the use of high-level language compilers. These methods are listed in increasing levels of abstraction, with schematic design entry being the lowest level.

4 Overview of Adaptive Filters

In practice, signals of interest often become contaminated by noise or other signals occupying the same band of frequency. When the signal of interest and the noise reside in separate frequency bands, conventional linear filters are able to extract the desired signal. However, when there is spectral overlap between the signal and noise, or the signal or interfering signal's statistics change with time, fixed coefficient filters are inappropriate Figure 4 shows an example of a wideband signal whose Fourier spectrum overlaps a narrowband interference signal.

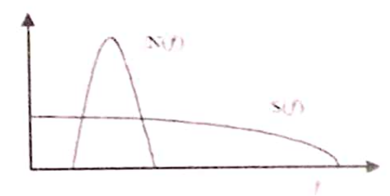

Fig. 4 Narrowband interference N (f) in a wideband signal S (f)

This situation can occur frequently when there are various modulation technologies operating in the same range of frequencies. In fact, in mobile radio systems co-channel interference is often the limiting factor rather than thermal or

other noise sources. It may also be the result of intentional signal jamming, a scenario that regularly arises in military operations when competing sides intentionally broadcast signals to disrupt their enemies' communications.
Furthermore, if the statistics of the noise are not known a priori, or change over time, the coefficients of the filter cannot be specified in advance. In these situations, adaptive algorithms are needed in order to continuously update the filter coefficients.

Adaptive Algorithms

There are numerous methods for the performing weight update of an adaptive filter. There is the Wiener filter, which is the optimum linear filter in the terms of mean squared error, and several algorithms that attempt to approximate it, such as the method of steepest descent. There is also least-mean-square algorithm, developed by Widrow and Hoff originally for use in artificial neural networks. Finally, there are other techniques such as the recursive-least-squares algorithm and the Kalman filter. The choice of algorithm is highly dependent on the signals of interest and the operating environment, as well as the convergence time required and computation power available.

Wiener Filters

The Wiener filter, so named after its inventor, was developed in 1949. It is the optimum linear filter in the sense that the output signal is as close to the desired signal as possible. Although not often implemented in practice due to computational complexity, the Wiener filter is studied as a frame of reference for the linear filtering of stochastic signals to which other algorithms can be compared.

Least-Mean-Square Algorithms

The least-mean-square (LMS) algorithmis similar to the method of steepest-descent in that it adapts the weights by iteratively approaching the MSE minimum. Widrow and Hoff invented this technique in 1960 for use in training neural networks. The key is that instead of calculating the gradient at every time step, the LMS algorithm uses a rough approximation to the gradient.

Recursive Least Squares Algorithm

The recursive-least-squares (RLS) algorithm is based on the well-known least squares method. The least-squares method is a mathematical procedure for finding the best fitting curve to a given set of data points. This is done by minimizing the sum of the squares of the offsets of the points from the curve. The RLS algorithm recursively solves the least squares problem.

FPGA Implementation

Field programmable gate arrays are ideally suited for the implementation of adaptive filters. However, there are several issues that need to be addressed. When performing software simulations of adaptive filters, calculations are normally carried out with floating point precision. Unfortunately, the resources required of an FPGA to perform floating point arithmetic is normally too large to be justified, and measures must be taken to account for this. Another concern is the filter tap itself. Numerous techniques have been devised to efficiently calculate the convolution operation when the filter's coefficients are fixed in advance. For an adaptive filter whose coefficients change over time, these methods will not work or need to be modified significantly.
First, the issues involved in transitioning to a fixed-point algorithm will be detailed. Next, the design of the filter tap will be considered. The reconfigurable filter tap is the most important issue for high performance adaptive filter architecture, and as such it will be discussed at length. Finally, the integration of the embedded

processor for the coefficient update will be discussed.

Embedded Microprocessors

The current trend in programmable logic is the inclusion of embedded DSP blocks and microprocessors. The Virtex-II Pro FPGA form Xilinx contains an embedded PowerPC 405 microprocessor, and numerous soft IP cores. To design for this environment the Embedded Development Kit must be used.

IBM Power PC 405

The IBM PowerPC 405 is a 32-bit RISC microprocessor embedded in Xilinx's Virtex-II Pro FPGA. The core occupies a small die area and consumes minimal power making it ideal for system-on-chip (SoC) embedded applications. It can run at a clock speed of over 400 MHz to produce over 600 Dhrystone MIPS. A memory management unit (MMU), a 64-entry unified Translation Look-aside Buffers (TLB), debug support, and watchdog timers enable an embedded operating system to function for no additional logic cost.

RESULTS

Several different implementations were tested, including hardware only designs as well as combined hardware/software embedded systems. This topic gives an overview of the hardware verification method, presents the implementation results, and compares them to the results from Matlab trials.

Full Precision Analysis

The application tested was adaptive noise cancellation, for reasons discussed in a previous topic. A sine wave is the desired signal, but is corrupted by a higher frequency sinusoid and random Gaussian noise with a signal to noise ratio of 5.865 dB. A direct form FIR filter of length 16 is used to filter the input signal. The adaptive filter is trained with the LMS algorithm with a learning rate $\mu = 0.05$. The filter is also trained with the RLS algorithm with the parameters $\delta = 1$ and $\lambda = 0.99$.

The floating-point precision results are presented. It appears that the filter trained with the LMS algorithm has learned the signals statistics and is filtering acceptable within 200 - 250 iterations. When trained with the RLS algorithm, the filters weights are near optimal within 50 training iterations, almost an order of magnitude faster, as expected.

Fixed Point Analysis

The above algorithms were converted so that all internal calculations would be done with a fixed-point number representation. This is necessary, as the embedded PowerPC has no floating-point unit (FPU), and FPGA's don't natively support floating-point either. Although a FPU could be designed in an FPGA, they are resource intensive, and therefore can feasibly only support sequential operations. Doing so however would fail to take full advantage of the FPGA's major strength, which is high parallelization.

The LMS and RLS algorithms were modified as detailed in Chapter 4, and a transposed representation of the LMS was also implemented. A scale of 256 with 16-bit precision was found to be suitable. The results of the fixed-point LMS algorithm were comparable to the full precision representation of the same algorithm. The RLS though, was considerably worse. The 16-bit fixed-point results are presented.

For a 16-bit fixed representation, the RLS algorithm displayed a significant degradation as compared to the algorithm represented with floating-point accuracy. It appears that the RLS algorithm is very sensitive to the internal precision used, and therefore its superiority over the LMS algorithm is diminished when a fixed representation is needed. In fact, considering the extra computation needed, the RLS algorithm is barely better, yet requires significantly more development time due to its complexity.

Because the error at the output of a transposed-form FIR filter is due to the accumulation of past inputs and weight, it converges much differently than the direct form FIR. The transposed LMS algorithm takes much longer to converge and never converges close enough. However, it may be suitable when absolute data throughput is necessary. The output of a fixed-point transposed form LMS algorithm after approximately 2500 iterations.

Power Consumption

When choosing between different designs for embedded applications, the power consumed by the device is an important issue. The power consumed by the different architectures. Designs utilizing the PowerPC microprocessor averaged 920 mW of power use, while designs using FPGA logic only averaged 757 mw. On average, the inclusion of the PowerPC uses 164 more mW than design without it.

CONCLUSIONS

A significant amount of design time was spent working out minor bugs and intricacies within the EDK software. In fact, the extra time spent debugging cancelled out the amount of time saved by coding in a high-level language. Hopefully, these bugs will be addressed in future software releases. In addition, reference designs provided by Avnet were used for the memory transfer to the SRAM through the PCI bus. Since the PCI bus and the PPC405 share the SRAM, a control bit and machine interrupt are used. This bit needed to be set manually during testing. It is unclear whether this is due to software or hardware errors. Until an appropriate fixed-point structure is found for the Recursive Least-Squares algorithm, the Least Mean-Square algorithm was found to be the most efficient training algorithm for FPGA based adaptive filters. The issue of whether to train in hardware or software is based on bandwidth needed and power specifications, and is dependent on the complete system being designed. While the extra power consumed would make the PowerPC seem unattractive, as part of a larger embedded system this could be practical. If many processes can share the PowerPC then the extra power would be mitigated by the creation of extra hardware that it has avoided. Furthermore, an area greatly simplified by the inclusion of a microprocessor is memory transfers. These are sequential in nature and within the EDK there are many memory IP modules. With no microprocessor, a finite state machine for timing, as well as a memory interface is needed, and these will consume more power, although still less than the PowerPC. Lastly, the microprocessor can be used to easily swap out software training algorithms for application testing and evaluation. Embedded microprocessors within FPGA's are opening up many new possibilities for hardware engineers, although it requires a new design process. The future of embedded Systems-on-Chip design will involve more precisely determining the optimal hardware and software tradeoffs for the functionality needed.

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Review Paper on Generation of Mobile Communication Technologies (1G to 5G)

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Abstract

Wireless technology is very much in demand these days. A newly wired network was needed to get online. Even wired telephones are becoming a thing of past. Nowadays, Mobile networks have full-blown tremendously in the last four decades. The inception was the Cellular concept which was introduced with 1G, where, 'G' stands for generation networks. It had grown so fast, from generation to generation, nurturing from 1G, 2G, 3G, and finally, launched to 4G. And, today, we are using 4G technologies. And, also, 5G technology is almost ready to spread its wings to storm this competitive global mobile network market. Integrated Research on 5G is being carried on and is expected to come in usage commercially by 2020. The birth of 5G technology can be an optimal solution to the various problems that we are facing in the current technologies nowadays. 5G will emerge as an intelligent technology that will reduce the number of different technologies to a single entity of a global standard. This paper is mainly focused on the development of mobile wireless communication network from 1G to 5G and how they are different from each other and their advantages and disadvantages they possess.

Key words- Wireless Technology, Wired telephone, Cellular concept,1G,2G,3G, 4Gand 5G.

INTRODUCTION

Over the most recent couple of decades, Mobile Wireless Communication systems have encountered a remarkable change. The mobile wireless Generation (G) for the most part alludes to an adjustment in the idea of the framework, speed, technology, frequency, data capacity, latency etc. Each generation has some standards, different capacities, new techniques and new features which separate it from the past one. The first generation (1G) mobile wireless communication network was analog utilized for voice calls only. The second generation (2G) is a digital technology and supported text messaging. The third-generation (3G) mobile technology provided higher data transmission rate, increased capacity and gave interactive media bolster. The fourth generation (4G) incorporates 3G with fixed internet to help wireless mobile internet, which is an advancement to mobile technology and it beat the limitations of 3G. there was an increase in the bandwidth and reduced the cost of resources [1]. 5G stands for fifth Generation mobile technology and will be unveiled as another unrest in a portable market which will change the way of utilizing cell phones within the very high bandwidth. A user will never experience ever before such high esteem technology which will incorporate all kinds of advanced features and 5G technology will be the most intense and in huge demand in the coming future.

EVOLUTION

Mobile communication had turned out to be well known in the most recent couple of years because of its quick change from 1G to 5G in the field of mobile technology. This change is because of the necessity of service compatible transmission technology and high increment in telecom clients. Basically, Generation refers to change in nature of service compatible transmission technology and new frequency bands. In 1980, for the first time the mobile cellular system was introduced, and since then, the mobile communications had experienced tremendous changes which pursued its vast sustainment.

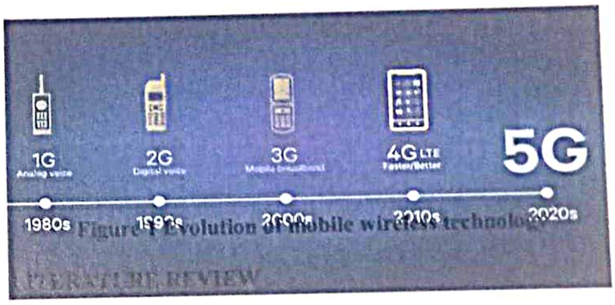


Figure 1 Evolution of mobile wireless technology

LITERATURE REVIEW

First Generation, 1G

These telephones were the first and the foremost cell phones to be utilized, which was presented in 1982 and finished in mid-1990. It was utilized for voice benefits and depended on the technology called Advanced Mobile Phone System (AMPS). The AMPS framework was frequency modulated and utilized the frequency division multiple access(FDMA) with a channel limited to 30 KHz and with a frequency band of 824- 894 MHz[5].

The primary highlights of 1G are:[20] Speed- 2.4 Kbps, Allows voice brings in one nation, Use analog signal, Poor voice quality, Poor battery life, Large phone measure, Limited capacity, Poor handoff unwavering quality, Poor security, and Offered low level of spectrum efficiency.

It presents Mobile Technologies, for example, Mobile Telephone System (MTS), Advanced Mobile Telephone System (AMTS), Improved Mobile Telephone Service (IMTS) and Push to Talk(PTT). It has low capacity, problematic hand-off, poor voice quality and no security at all since voice gets back to were played in radio towers, making these calls helpless to undesirable in listening stealthily by outsiders.[1]
The main drawback of 1G technology is that it uses analog signals rather than digital signals, this is less effective means of transmitting information, it is slower, and the signals cannot reach as far in terms of secluded areas so 2G is coming to overcome these problems.

Second Generation (2G)

2G alludes to the second generation based on GSM and was developed in the late 1980s. It utilizes digital signals for voice transmission. Fundamental concentrate of this technology was on digital signals and gives services to convey content and provide picture message at low speed (in kbps). It utilized the bandwidth of 30 to 200 KHz. Three types of developments took place in second generation wireless communication system, IS-54(TDMA) in 1991, IS-95(CDMA) in 1993, and IS-136 in 1996. Besides 2G, 2.5G framework utilizes packet switched and circuit switched domain and gave data rate up to 144 kbps example GPRS, CDMA, and EDGE [5].

The primary highlights of 2G and 2.5G are [20] Data speed was up to 64 kbps, Use digital signals, Enables services, for example, instant messages, picture messages and MMS (Multimedia message), Provides better quality and capacity, Required solid digital signals to enable cell phones to work. On the off chance that there is no network coverage in any particular range, digital signals would frail, Need to enhance
transmission quality, Spotty coverage, Unfit to help complex data for example video, System capacity, Cell towers has a constrained coverage region, and Unexpected dropped calls.

The GSM Technology was persistently enhanced to give better services which prompted improvement of advanced technology between 2g and 3g. Provides phone calls, Send/ get email messages, Web browsing, Speed: 64-144 kbps, Camera cell phones, and Take a period of 6-9 mins. To download a 3 min. MP3 tune.[20]Weaker digital signal is one of the main disadvantage of 2G technology to overcome this problem 3G technology is coming.

Third Generation (3G)
3G depends on GSM and was propelled in 2000. The point of this technology was to offer high-speed data. The first technology was enhanced to permit data up to 14 Mbps and additionally utilizing packet switching. It utilizes Wide Band Wireless Network with which lucidity is enhanced. It likewise offers data services, access to TV/ video, new services like Global Roaming. It works at a range of 2100 MHz and has a bandwidth of 15-20 MHz utilized for high- speed web access, video chatting [5].
The primary highlights of 3G are:[20] Speed 2Mbps, Typically called advanced mobile phones, Increased bandwidth and data transfer rates to oblige web-based applications and furthermore, video documents, Provides quicker communication, Send/get expansive email messages, High speed web/ greater security/ video conferencing/ 3D gaming., Large capacities and broadband capabilities, TV streaming/ Mobile TV/ Phone calls, To download a 3 minute MP3 tune just 11 sec-1.5 minutes time required, Expensive charges for 3G licenses services, It was test to assemble the frame work for 3G, High bandwidth required, Expensive 3G phones, and Large cell phones.

The 3G mobile system was called as UMTS (Universal Mobile Telecommunication System) in Europe, while CDMA 2000 is the name of American 3G variant. Additionally, the IMT 2000 has acknowledged another 3G standard from China, i.e. TD-SCDMA.
WCDMA is the air-interface technology for UMTS [1].
The service provider has to pay the high amount for 3G licensing & agreements, the problem with the availability of handsets in few regions and their costs, 3G networks need different devices and the power consumption is high is the main disadvantages of 3G to overcome this 4G is coming.

Fourth Generation (4G)

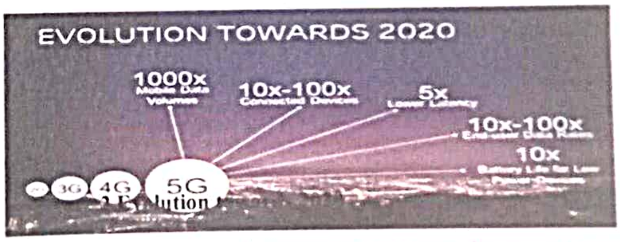
A term MAGIC is used to explain the 4G technology [9]. M= mobile multimedia

A= any time any where G= global mobility support
I= integrated wireless solution C= customized personal service
4G wireless technology should put together different presently existing and prospect wireless network technologies (e.g. OFDM, MC-CDMA, LAS-CDMA and Network- LMDS) to make sure that free movement and faultless roaming from one technology to another is achieved [10].

4G offers a downloading speed of 100 Mbps. 4G gives same features as 3G and extra services like multi-media newspapers, to watch television programs with greater clearness and send data substantially speedier than past generations[3].

LTE (Long-term evolution) is considered as 4G technology. 4G is being created to accommodate the QoS and rate requirements set by expected applications like wireless broadband access, Multi-media Messaging Service (MMS), video chat, Mobile TV, HDTV content, Digital Video Broadcasting (DVB), minimal services like voice and data and different services that use bandwidth [2].
The fundamental highlights of 4G are: [20] Capable of give 10Mbps-1Gbps speed, High quality streaming video, Combination of Wi-Fi and Wi-Max, High security, Provide any sort of service whenever according to user necessities anyplace, Expanded multi-media services, Low cost per-bit, Battery consumption is more, Hard to implement, Need convoluted hardware, and Expensive equipment required to actualize next generation network
Obtaining the information from the people illegally becomes easier, the 4G technology involves the possibility of some interference though not much, It is capable of being attacked (jamming frequencies) and the invasion of the privacy increased. The consumer is forced to buy a new device to support the 4G , New frequencies
means new components in the cell towers, Higher data prices for the consumers, Your current equipment cannot be compatible with the 4G network , It has different network bands for different phones It is expensive & hard to implement .4G technology requires expensive infrastructure for operation , This is embodied in the eNodeB's (Access Points) & mainly EPC's (Gateways or Routers), 4G is optimal for data rates , but not necessarily the best for Voice services , Some of these services are offloaded (delegated) to Wi-Fi or 3G/GSM cellular technologies on your phone. To overcome the above disadvantages of 4G, 5G is coming.

REQUIREMENT FOR FIFTH GENERATION WIRELESS COMMUNICATION SYSTEM



As a customer point of perspective, the main divergence among present generations and coming 5G techniques ought to be as per the following[12]:Lower latency, To help gadgets in the internet of things, Higher capacity then 4G, Latency decreased fundamentally contrast with LTE, Enhanced coverage, Concurrent vast number of connections for wireless sensors, Data rates approx 100Mbps, Improved signalling efficiency, Enhanced and creative data coding techniques, Millimeter waves frequencies for wireless access and back haul utilize, Smart beam antenna systems, Bring down blackout problem, Not destructive for well being, Less expensive traffic charges, World Wide Wireless web, More secure and SDR security, Lower battery utilizations, Numerous simultaneous data exchange ways, and Accommodating being used of artificial intelligent in human life for securing communications
Above examined brings up out the requirements for 5g. The fifth generation is to be another technology that will give all the available applications, by using just a single worldwide device and joining about the whole already alive communication infrastructure. Fifth generation stations will be empowered of an unlikely multimode and cognitive radio. The fifth-generation cellular networks will accentuation on the advancement of the user

stations where stations will have passage to different wireless technologies at the same time and will combine different issues from different technologies. Also, the station will make the best choice between different wireless/cellular access network providers for likely service [13].

5G technology will be deployed by 2020. It provides the great feature to users, having higher data rate 1Gbps or higher. 5G support 4G+WWWW (4th Generation +Wireless World Wide Web). It operates on IPv6 protocol. Fifth generation technology utilizes CDMA and BDMA and millimeter wireless which approves speed is higher than 100Mbps at full speed and more prominent than 1Gbps at low speed. The fifth-generation networks work on encoding type known as OFDM [11]. 5G aim to provides unlimited access and information at anywhere anytime with high speed. It is a complete wireless communication with no limitations. The fundamental highlights of 5G are:[20]

It is exceptionally supportable to WWWW (wireless world wide web), High speed, high capacity, Provides substantial broadcasting of data in Gbps, Multi-media newspapers, watch TV programs with the clarity (HD clarity), Faster transmission that of the previous generation, Large phone memory, dialing speed, lucidity in sound/video, Support intelligent multimedia, voice, streaming video, web and other, and More successful and appealing.

Table 1. Correlation of Mobile Generation: 1G To 5G

Technology	1G	2G	3G	4G	5G
Start/Deployment	1970-80	1990-2004	2004-2010	Now	Soon(probably by 2020)
Data Bandwidth	2 Kbps	64 Kbps	2Mbps	1Gbps	Higher than 1 Gbps
Technology	Analog	Digital	CDMA 2000, UMTS,EDGE	Wi-Max, Wi-Fi, LTE	WWWW
Core Network	PSTN	PSTN	Packet N/W	Internet	Internet
Multiplexing	FDMA	TDMA/CDMA	CDMA	CDMA	CDMA
Switching	Circuit	Circuit, Packet	Packet	All Packet	All Packet
Primary Services	Analog phone cells	Digital phone calls and messaging	Phone calls, messaging, data	All- IP Service(including voice messages)	High speed, high capacity and provide large broadcasting of data in Gbps
Key differentiator	Mobility	Secure, Mass Adoption	Better Internet Experienc e	Faster broadband internet, lower latency	Better coverage and no dropped calls, much lower latency, better performance
Weakness	Poor spectral efficiency, major security issues	Limited data rates, difficult to support demand for internet and e-Mail	Real works fail to match type, failure of WAP for internet access	Battery use is more, required complicated and expensive hardware	?

CONCLUSION

Mobile has become the essential part of our everyday life. Their current development is the outcome of various generations. In this paper we review the various generations of mobile wireless technology, their technologies use in various generations, performance, advantages, and disadvantages of one generation over other

and comparison. This field is still full of research opportunities and research on upcoming technology 5G is carry on which is coming in 2020.

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