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Editorial

Radio over Fiber is an upcoming wireless standard which is being designed to seamlessly integrate many different standards as well as integrate broadband communication wirelessly. As the technology is improving so are the demands of end users and their applications increasing. A wide variety of new applications are being invented daily. These applications have different demands from the underlying network protocol suite. Several issues need to be taken into account while considering a wireless network. Quality of service (QoS) is one of the most important among all.

Decoding of LDPC block codes over Convolutional codes with channels have been shown to be capable of achieving the same capacity-approaching performance as LDPC block codes with iterative message-passing decoding. However, for comparing block and convolutional codes tied to the implementation complexity of trellis based decoding are irrelevant for message-passing decoders. Complete-MDP convolutional codes perform in many cases better than comparable MDS block codes of the same rate over the erasure channel.

A new high gain, multiband hexagonal-shape slot loaded microstrip patch antenna is printed on a dielectric substrate, backed by a metal board, and directly fed from a 50 Ω coaxial cable. The introduction of rectangular slot in hexagonal antenna offers a low profile, multiband, high gain and compact antenna.

In Wireless Mobile Cellular Networks, users usually move between heterogeneous networks. In this type of environment, handoff procedure algorithm, handoff decision and its management is very important issue. Wireless Mobile Cellular Network supports the handoff process for users between various wireless technologies such as WLAN, CDMA and modern 3G networks.

Preface

Dear Researchers,

We take this opportunity to welcome you all to the Volume No 3, Issue No. 1 of International Journal of Communications & Electronics (KIET - IJCE). This journal will provide a forum for in depth and substantial discussions on the theory, design and implementation of the emerging technologies in Communications, Networking, Microwave and Electronics techniques, thus providing solutions and strategies for business resilience.

It gives us an immense pleasure to have an amalgam of researchers from the fields of Communication Engineering, Electronics, and related technologies. The purpose of the Journal is to provide a platform to foster interdisciplinary communication among the delegates and to support the sharing process of diverse fields in various concepts and principles related to these domains.

Our appreciation also goes to entire team whose dedication and timeless efforts have gone for number of days for the second issue of the Journal.

Editors

Message

I am delighted to note that the Department of Electronics and Communication Engineering, KIET Group of Institutions, Ghaziabad is introducing Volume No 3, Issue No. 1 of International Journal of Communications and Electronics (KIET - IJCE).

I appreciate the efforts on the part of the Editorial Committee in bringing out an issue on Communications, Networking, Microwave and Electronics techniques.

I understand that the papers contributed for publication in the Volume No 3, Issue No. 1 are on almost all the current aspects of Communication Systems, Electronics systems, Microwave Engineering, Signal Processing & Applications, Networking Technologies and several others.

I have great pleasure in congratulating the Editors of this issue of KIET - IJCE for their untiring efforts in bringing out this third Volume No 3, Issue No. 1 of KIET-IJCE which will be a valued treasure for all who pursue research in Communications, Networking, Microwave and Electronics Engineering areas. .

Let me close with warmest regards.

Dr. Sraban Mukherjee
Director
KIET

Message

It gives me immense pleasure in writing this foreword for the Volume No 3, Issue No.1 of the KIET International Journal on Communications and Electronics (KIET - IJCE). This journal is targeted towards researchers, professionals, educators and students to share innovative ideas, issues, recent trends and future directions in the fields of Electronics and Communication Engineering.

The Volume No 3, Issue No. 1 of the journal KIET-IJCE includes papers on the theory, design and implementation of the emerging technologies in the field of Communications, Networking, Microwave and Electronics techniques. Furthermore, it will enable the researchers in various domains to foster the exchange of concept, protypes, research ideas and the results of research work which could contribute to the academic arena and also befit business and industrial community.

Dr. Sanjay Sharma
Editor – in - chief
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Decoding of LDPC Block Codes overConvolutional Codes with Channels

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***Abstract*–Decoding of LDPC block codes over Convolutional codes with channels have been shown to be capable of achieving the same capacity-approaching performance as LDPC block codes with iterative message-passing decoding.However, for comparing block and convolutional codes tied to the implementation complexity of trellis based decoding are irrelevant for message-passing decoders. In this paper, we shows a comparison of LDPC block and convolutional codes based on several factors.In this paper the erasure channel are studied. Of special interest will be maximum distance profile (MDP) convolutional codes. These are codes which have a maximum possible column distance increase.This is shown how this strong minimum distance condition of MDP convolutional codes help us to solve error situations that maximum distance separable (MDS) block codes fail to solve. For this, two subclasses of MDP codes are defined: reverse-MDP convolutional codes and complete-MDP convolutional codes. Reverse-MDP codes have the capability to recover a maximum number of erasures using an algorithm which runs backward in time. Complete-MDP convolutional codes are both MDP and reverse-MDP codes. They are capable to recover the state of the decoder under the mildest condition.It is shown that complete-MDP convolutional codes perform in many cases better than comparable MDS block codes of the same rate over the erasure channel.**

***Index Terms*—Convolutional codes, maximum distance separable (MDS) block codes, decoding, erasure channel,maximum distance profile (MDP) convolutional codes, reverse-MDP convolutionalcodes, complete-MDP convolutional codes. maximum distance profile (MDP) convolutional codes, reverse-MDP convolutionalcodes.**

I. INTRODUCTION

As an erasure channel is transmitting, one of the problems encountered is the delay experienced on the received information due to the possible re-transmission of lost packets. One way to eliminate these delays is by using forward error correction. After the invention of turbo codes, researchers became aware that Gallager's low-density parity check (LDPC) block codes [1], were also capable of capacity-approaching performance on a variety of channels. Low-density parity-check (LDPC) codes, although introduced in the early 1960's [20], were established as stateof-the-art codes only in the late 1990's with the application of statistical inference techniques [21] to graphical models representing these codes [22], [23]. The promising results from LDPC block codes encouraged the development of convolutional codes defined by sparse parity-check matrices.Analysis and design of these codes quickly attracted considerable attention in the literature, beginning with the work of Wiberg [2], MacKay and Neal [3], and many others.The convolutional counterparts of LDPC block codes, namely LDPC convolutional codes, were subsequently proposed in [4].Analogous to LDPC block codes, LDPC convolutional codesare defined by sparse parity-check matrices that allow them to be decoded using a sliding window-based iterative message passing decoder. The use of convolutional codes over the erasurechannel has been studied much less.Recent studies have shown that LDPC convolutional codes are suitable for practical implementation in a number of different communication scenarios, including continuous transmission as well as block transmission in frames of arbitrary size [5], [6], [7].In this paper, we define a class of convolutional codes with strong distance properties, which we call complete maximum distance profile (complete-MDP) convolutional codes, and we demonstrate how they provide an attractive alternative. They are also known for their encoding simplicity,since the original code construction method proposed in [4] yields a shift-register based systematic encoder for real time encoding of continuous data. This is an advantage when compared to randomly constructed LDPC block codes.Given their excellent bit error rate (BER) performance along with their simplicity ofencoding,

it is quite natural to compare LDPC convolutional codes with corresponding LDPC block codes. In this paper, we compare these codes under several different assumptions: equal decoding computational complexity, equal decoding processor (hardware) complexity,equal decoding memory requirements, and equal decoding delay.

The paper is organized as follows. In Section II, we provide a brief overview of LDPC convolutional codes. The maincontribution of the paper is Section III, where comparisonsof LDPC block and convolutional codes based on severalcriteria are presented. In the next section, we focus on finiteblock length comparisons between LDPC block codes andterminated LDPC convolutional codes. Finally, we providesome conclusions in Section V.

II. AN LDPC CONVOLUTIONAL CODES

Here defines the LDPC-CC as a rate R = b/c binary, time-varying LDPC-CC is definedas the set of semi-infinite binary row vectors v[∞] satisfying equation $vH^T=0$. An (m_s; J;K) regular LDPC convolutional code is the setof sequences v satisfying the equation $vH^T= 0$, where

$$H^T=\begin{pmatrix} H_0^T(0) & \cdots & H_{m_s}^T(m_s) & & \\ & \ddots & & & \\ & H_0^T(t) \ldots & H_{m_s}^T(t+m_s) & & \end{pmatrix} \ldots(1)$$

As the given parameter m_s is called the memory of the code and $v_s = (m_s + 1)$ c is referred to as the constraint length$H^T$is the (time-varying) semi-infinite syndrome former (transposed parity-check) matrix. For a rate R = b/c, b < c, LDPC convolutional code, the elements $H^T_i(t)$, i =0,1,2,3,...m_s are binary c X (c - b) sub matrices defined as

$$H_i^T(t)=\begin{bmatrix} h_i^{(1,1)}(t) & \cdots & h_i^{(1,c-b)}(t) \\ \vdots & \ddots & \vdots \\ h_i^{(c,1)}(t) & \cdots & h_i^{(c,c-b)}(t) \end{bmatrix} \ldots(2)$$

Starting from the m_s (c - b)th column, H^Thas J ones in each row and K ones in each column. The value ms,called the syndrome former memory, is determined by themaximal width of the nonzero area in the matrix H^T, and the associated constraint length is defined as.v_s= (m_s +1) c. In practical applications, periodic syndrome former matricesare of interest. Periodic syndrome formers are said to have a period T if they satisfy $H_i^T(t) = H_i^T(t+T)$, i=0, 1,.m_s

The advantage that convolutional codes to blockcodes, which will be exploited in our algorithms, is the flexibilityobtained through the "sliding window" characteristic ofconvolutional codes. The received information can be groupedin appropriate ways, depending on the erasure bursts, andthen be decoded by decoding the "easy" blocks first. Thisflexibility in grouping information brings certain freedom inthe handling of sequences; we can split the blocks in smallerwindows, we can overlap windows and we can proceed todecode in a less strict order.

Although the corresponding Tanner graph has an infinitenumber of nodes, the distance between two variable nodes that are connected to the same check node is limited by the syndrome former memory of the code. This allows continuous decoding that operates on a finite window sliding along the received sequence, similar to a Viterbi decoder with finite path memory [8]. The decoding of two variable nodes that are at least (m_s+1) time units apart can be performed independently, since the corresponding bits cannot participate in the same parity-check equation. This allows the parallelization of thel iterations by employing I independent identical processors working on different regions of the Tanner graph simultaneously. Alternatively, since the processors implemented in the decoder hardware are identical, a single .hopping. Processor that runs on different regions of the decoder memory successivelycan also be employed. A pipeline decoding architecture that is based on the ideas summarized in the previous paragraph was introduced by Jimenez Felstrom and Zigangirov in [4]. The pipeline decoderoutputs a continuous stream of decoded data once an initial decoding delay has elapsed. The operation of this decoder on the Tanner graph for a simple time-invariant rate R = 1/3 LDPC convolutional code with m_s = 2 is shown in Figure 1. (Note that, to achieve capacity-approaching performance, an LDPC convolutional code must have a large value of m_s) .

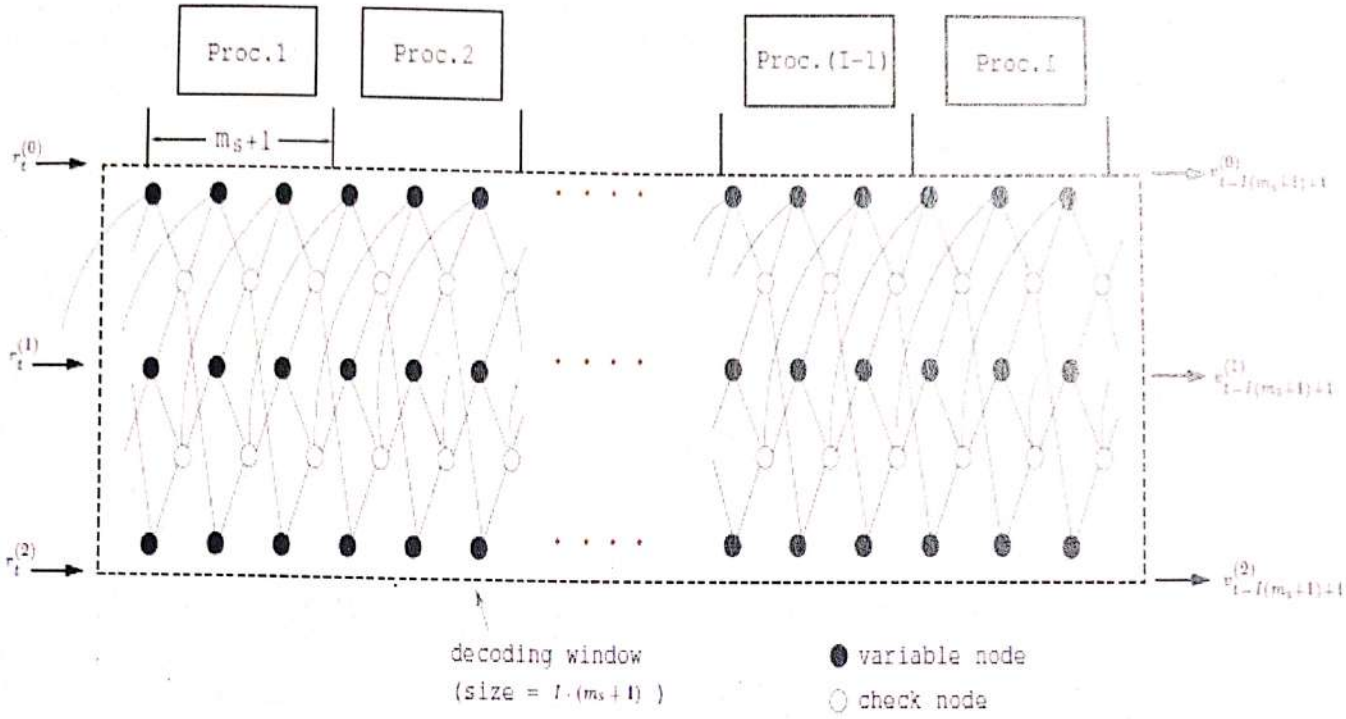

Fig. 1. Tanner graph of an R=1/3 LDPC convolutional code and an illustration of pipeline decoding.

III. COMPARISONS OF LDPC BLOCK AND CONVOLUTIONAL CODES WITH AN IMPLEMENTATION

Here, we compare several aspects of decoding LDPC convolutional and block codes.

A. Complexity With Computational Methodology

Let C_{check} (C_{var}) denote the number of computations required for a check (variable) node update for a check (variable) node of degree N (M). Regardless of the code structure, C_{check}andC_{var}only depend on the values M and N. For a rate R = b/c, (m_s; M, N)-LDPC convolutional code decoded using a pipeline decoder with I iterations/processors,at every time instant each processor activates c - b check nodes and c variable nodes. The computational complexity per decoded bit is therefore given by

$$C_{bit}^{conv} = \left((c-b).C_{check} + c.C_{var}\right).\frac{I}{c} \ldots (3)$$
$$= \left((c-b).C_{check} + c.C_{var}\right).I$$

which is independent of the constraint length v_s.Similarly, the decoding complexity for an (L,M,N)-LDPCblock code is given by

$$C_{bit}^{block} = (L.M/N.C_{check} + L.C_{var}).1/L) \ldots (4)$$
$$= (M/N.C_{check} + C_{var}).I$$
$$= ((1-R).C_{check} + C_{var}).I$$

which is again independent of the code length L. Thus, thereis no difference between block and convolutional LDPC codeswith respect to computational complexity.

B. Processor (Hardware) Complexity

The sliding window decoder implementation of an LDPCconvolutional code operates on I v_s symbols. Howeverdecoding can be carried out by using I identical independentparallel processors, each capable of handling only $v_s$symbols. Hence it is sufficient to design the processor hardware for v_s symbols. For an LDPC block code of length L, the processor must be capable of handling all L symbols. Therefore, forthe same processor complexity, the block length of an LDPCblock code must be chosen to satisfy $L = v_s$

C. Memory Requirements

For the pipeline decoder, we need a storage element foreach edge in the corresponding Tanner graph. Each variablenode also needs a storage element for the channel value. Thusa total of I. (M + 1) $v_s$storage elements are required for literations of decoding. Similarly, we need L (M +1) storageelements for the decoding of an LDPC block code of lengthL. Thus,

for the same memory requirements, an LDPC blockcode must satisfy $L = I.v_s$

D. Decoding Delay

Let T_{ss} denote the time between the arrival of successivesymbols, i.e., the symbol rate is $1=T_{ss}$. Then the maximumtime from the arrival of a symbol until it is decoded is givenby

$$\Delta_{io}^{conv} = ((c-1) + (m_s + 1)c.I)T_{ss} \ldots\ldots (5)$$

The first term (c - 1) in (5) represents the time between the arrival of the first and last of the c encoded symbols output by arate R = b/c convolutional encoder in each encoding interval. The dominant second term (m_s + 1) .c. I is the time eachsymbol spends in the decoding window. Since c symbols areloaded into the decoder simultaneously, the pipeline decoderalso requires a buffer to hold the first (c - 1) symbols.

With LDPC block codes, data is typically transmitted ina sequence of blocks. Depending on the data rate and theprocessor speed, several scenarios are possible. We considerthe best case for block codes, i.e., each block is decoded bythe time the first bit of the next block arrives. This results ina maximum input-output delay of$\Delta_{io}^{block} = K.T_{ss}^{1}$.Thus, for equal decoding delays, the block length must satisfy L =(c - 1) + v_s. I, assuming the least possible delay for blockcodes.

E. VLSI implementation requirements

As previously noted, both LDPC block and convolutionalcodes can be decoded using message passing algorithms.Therefore decoder implementations in both cases consist ofidentical processing elements, namely variable nodes andcheck nodes. What differs between the two decoders is thetotal number of these elements and the way in which they areinterconnected.It is well known that VLSI implementations of parallelLDPC block decoders suffer from an interconnection problem[9]. This is due to the fact that processing nodes must be placed on the silicon at specific locations and connected as definedby H. Regardless of how the rows and columns of H arepermuted, long interconnections are still required. The sameobservation was also noted for LDPC block codes constructedusing algebraic techniques [10].However, VLSI implementations of LDPC convolutionaldecoders are based on replicating identical units, termedprocessors. As illustrated in Fig. 2, the complete decoder canbe constructed by concatenating a number of these processorstogether. For comparable BER performance, the size of anLDPC convolutional code processor needs to be about an orderof magnitude less than the block length of an LDPC block code[11]. Therefore the routing complexity within a processor is also an order of magnitude less than for a block code.

There is a wealth of other considerations than impact upon VLSI implementations of LDPC codes. These include the following.

- Any fully parallel LDPC block code decoder may suffer from routing congestion [9]. If so, the total area of such a decoder will be quite large and the maximum clock frequency will be limited by wiring delays.
- The fully parallel LDPC block code decoder can be replaced with a smaller decoder that implements a fraction of the circuit per clock cycle over a number of cycles. This reduces power, area, and throughput in a linear fashion.
- The LDPC convolutional code architecture is more amenable to pipelining because it is inherently feedforward architecture. Therefore it may achieve higher clock speeds.
- Since LDPC convolutional code decoders require fewer check and variable processing elements, the marginal cost of optimizing their critical paths in return for increasing their area is less than for LDPC block codes.
- Memory-based architectures have been proposed for both LDPC block codes [12] and LDPC convolutional codes [13].
- Algebraic code construction techniques can simplify LDPC block code decoder implementations [14], [15]. However since LDPC convolutional codes can often be constructed using the same methods these benefits may be applied to both types of codes [11].
- The choice may be affected by system level issues such as variable frame size, variable code rates, latency budgets, and target frame error rate (FER).

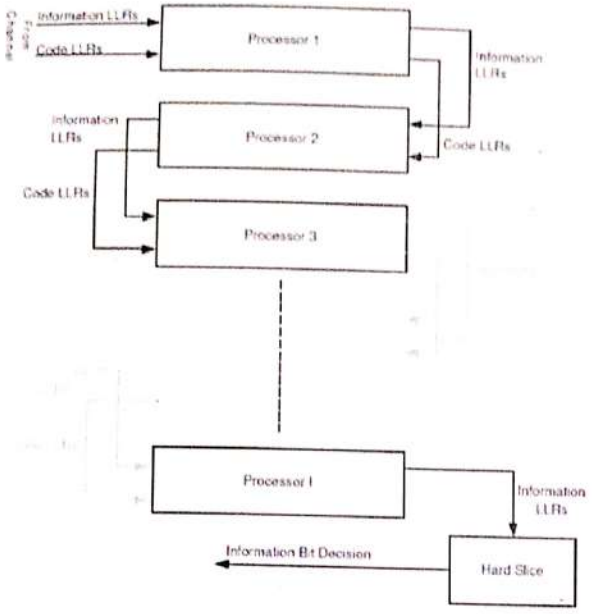

Fig. 2. LDPC convolutional code decoders can be implemented by concatenatingsub-units termed processors.

In Table I we present a brief summary of some existingLDPC block code and LDPC convolutional code VLSI implementations.In [16] a 54 MBPS decoder was implementedon a Xilinx Virtex-E FPGA. In [9] the decoder throughputwas much higher (500 MBPS) because the design was implementedas an ASIC. The BER was about $2X10^{-5}$ at 2dB. The decoder presented in [10] targets the IEEE 802.3anstandard [17], but it is a hard-decision decoder. This permits avery high throughput but compromises performance. Also note that the codes in [12] and [10] are high-rate, which makes iteasier to achieve higher throughput since less processing isrequired per information bit. The decoder presented in [7] isfor a very powerful LDPC convolutional code, and as such itachieves very good performance at the cost of relatively highcomplexity and low throughput. In [18] the first ever LDPCconvolutional code ASIC decoder is presented. It occupiesthree times less area (in a larger process) than the LDPCblock code ASIC in [9], however it has about three times lessthroughput and the BER performance is worse.The discussion in this section illustrates the point thatmaking a comparison between LDPC block codes and LDPCconvolutional codes that includes BER/FER performance andVLSI implementation complexity is not simple. It depends oncode choice, throughput, power, area, clock speeds, processingnode sizes, and system considerations. It is very possible thatthere is no single best choice between LDPC block codesand LDPC convolutional codes. Instead, LDPC block codesand LDPC convolutional codes may provide complementarysolutions and the appropriate choice may vary from one systemto another. It is worth noting that LDPC block codes havebeen the focus of extensive research for several years whereasLDPC convolutional codes are relatively understudied. The first attempts to implement decoders for LDPC convolutionalcodes noted here are encouraging enough to suggest thatfurther investigation is warranted.

IV. BER-FER PERFORMANCE COMPARISON OF LDPCBLOCK AND CONVOLUTIONAL CODES

In order to test the comparisons given in the previous section, in Figure 3 we plot the performance of a rate R = 1/2,(2048,3,6)-LDPC convolutional code with I = 50 iterationson an AWGN channel. Also shown is the performance of twoM = 3, N = 6 LDPC block codes with a maximum of 50iterations. The block lengths were chosen so that in one casethe decoders have the same processor complexity, i.e., L = $v_s$and in the other case the same memory requirements, i.e., L = v_s .I. For the same processor complexity, the convolutionalcode outperforms the block code by about 0.6 dB at a biterror rate of 10^{-5}. For the same memory requirements, theconvolutional and block code performance is nearly identical.LDPC convolutional codes are very efficient for the transmissionof streaming data since they allow continuous encodingdecoding. However, in some applications, it is preferable to have the data encoded in frames of pre-determined size in order to maintain compatibility with some standard format. Therefore, we now consider the performance of terminated LDPC convolutional codes in this context.

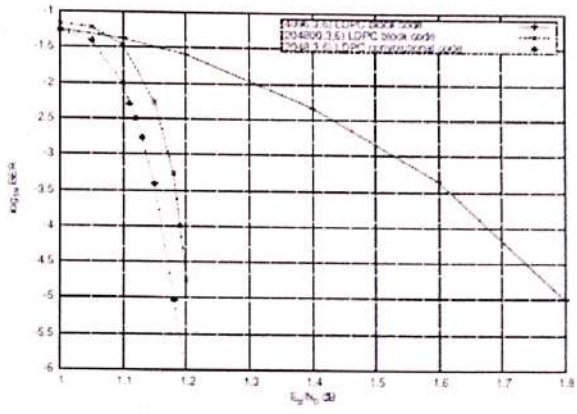

Fig. 3. BER performance comparison of LDPC block and convolutionalcodes.

The information sequence must be terminated with a tail ofsymbols to force the encoder to the zero state at the end of theencoding process. For conventional

polynomial convolutionalencoders, the terminating tail consists of a sequence of zeros.For LDPC convolutional code encoders, the tail is, generallyspeaking, non-zero and depends on the encoded informationbits. Therefore, a system of linear equations must be solved[19].

In Figure 4, we show FER performance comparisons ofterminated LDPC convolutional codes versus LDPC blockcodes, assuming 100 decoding iterations. We terminate a rateR = 1=2 (2048; 3; 6) LDPC convolutional code at variousframe lengths, resulting in a variety of terminated blocklengths and rates. We also provide simulation results for LDPCblock codes of comparable block lengths. As shown in Figure4, a single LDPC convolutional code can be employed toconstruct a family of codes of varying frame length and errorperformance via termination. This is an advantage in terms of flexibility compared to LDPC block codes, where a newcode must be constructed each time a new transmission framelength is required.

Figure 4 also shows that, even though the LDPC convolutionalcode with syndrome former memory m_s = 2048 has ahardware complexity comparable to that of a length L = 4096LDPC block code, its performance is similar to much longerLDPC block codes. In particular, for a terminated frame lengthof L = 64512, the LDPC convolutional code outperforms theLDPC block code of length L = 10000 and performs almostas well as the LDPC block code of length L = 100000.

V. ERASURE CHANNELS WITH MEMORY

We now consider the performance of LDPC-CC ensemblesand codes over erasure channels with memory. We considerthe familiar two-state Gilbert-Elliott channel (GEC) [32], [33]as a model of an erasure channel with memory. In this model,the channel is either in a "good" state G, where we assume theerasure probability is 0, or in an "erasure" state E, in whichthe erasure probability is 1. The state process of the channel isa first-order Markov process with the transition probabilitiesP{E→G}=gand P{G→E}=b. With these parameters,we can easily deduce [34] that the average erasure rate ε and the average burst length Δ are given by

$$\varepsilon = P\{E\} = \frac{b}{b+g}, \quad \Delta = 1/g$$

We will consider the GEC to be parameterized by the pair(ε, Δ). Note that there is a one-to-one correspondence betweenthe two pairs (b, g) and(ε, Δ).

Discussion: The channel capacity of a correlated binaryerasure channel with an average erasure rate of " is given as(1-ε), which is the same as that of the memoryless channel,provided the channel is ergodic. Therefore, one can obtaingood performance on a correlated erasure channel through theuse of a capacity-achieving code for the memoryless channel with an interleaver to randomize the erasures [24], [27]. This isequivalent to permuting the columns of the parity-check matrixof the original code. We are not interested in this approachsince such permutations destroy the convolutional structure of the code and as a result, we are unable to use the WD forsuch a scheme.

Construction of LDPC block codes for bursty erasure channelshas been well studied. The performance metric of acode over a bursty erasure channel is related to the maximumresolvable erasure burst length (MBL) denoted Δ_{max} [27],which, as the name suggests, is the maximal length of a singlesolid erasure burst that can be decoded by a BP decoder.Methods of optimizing codes for such channels therefore focuson permuting columns of parity-check matrices to maximizeΔ_{max}, Instead of permuting columns of theparity-check matrix, in order to maintain the convolutionalstructure of the code, we will consider designing $C_m(J;K)$ensembles that Δ_{max}.

A. Asymptotic Analysis

1) BP: As noted earlier, the performance of LDPC-CC ensemblesdepends on stopping sets. The structure of protographsimposes constraints on the code that limit the stopping set sizesand locations, as will be shown shortly.

Let us define a protograph stopping set to be a subsetS(B) of the VNs of the protograph B whose neighboringCNs are connected at least twice to S(B). These are alsodenoted as S(P), in terms of the set of polynomials definingthe protograph. We define the size of the stopping set asthe cardinality of S(B), denoted $|S(B)|$. We call the leastnumber of consecutive columns of B that contain the stopping set S(B) the span of the stopping set, denoted hS(B)i. Letus denote the size of the smallest protograph stopping setof the protograph B by |S(B)|*, and the minimum numberof consecutive columns of the protograph B that contain aprotograph stopping set by <S(B)>*. When the protographunder consideration is clear from the context, we will drop itfrom the notation and use $|S|$* and$\langle S \rangle$*. The minimum spanof a stopping set is of interest because we can give simplebounds for Δ_{max}based on <S(B)>*. Note that the stoppingset of minimal size and the stopping set of minimal span arenot necessarily the same set of VNs. However, we always have

$|S(B)|^* \leq \langle S(B) \rangle^*$.

TABLE I
A COMPARISON OF EXISTING BLOCK AND CONVOLUTIONAL LDPC CODE IMPLEMENTATIONS.NOTE PERFORMANCE FIGURES, WHERE AVAILABLE, AREGIVEN AT A CERTAINEb / N0

Ref.	Type	Code Params.	Code rate	Device	Perf.	Throughput
[9]	Block	(1024,3,6)	0.5	52.5mm^2 in 0.16µmCMOS	BER=2e^{-5}@2dB	500MBPS
[16]	Block	(9216,3,6)	0.5	FPGA	BER=1.0e^{-6}@2dB	54MBPS
[12]	Block	(8176,7154)	0.875	FPGA	N/A	169MBPS
[10]	Block	(2048,1723)	0.875	17.6mm^2 in 0.18µmCMOS	BER=5e^{-5}@6dB	3200MBPS
[13]	Conv.	(128,3,6)	0.5	FPGA	BER=1e^{-3} (1e^{-4})@2dB	75MBPS(25MBPS)
[7]	Conv.	(2048,3,6)	0.5	FPGA	BER=1e^{-10}@2dB	2MBPS
[18]	Conv.	(128,3,6)	0.5	16mm^2 in 0.18µm CMOS	BER=3e^{-4}@3dB	150MBPS

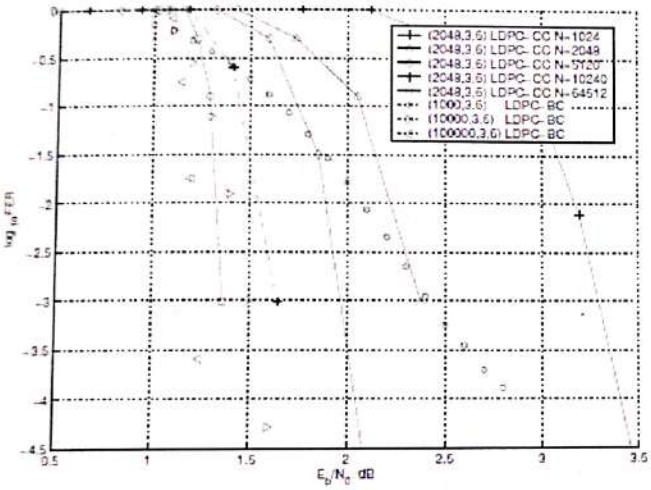

Fig. 4. FER performance comparison of terminated LDPC convolutional andblock codes.

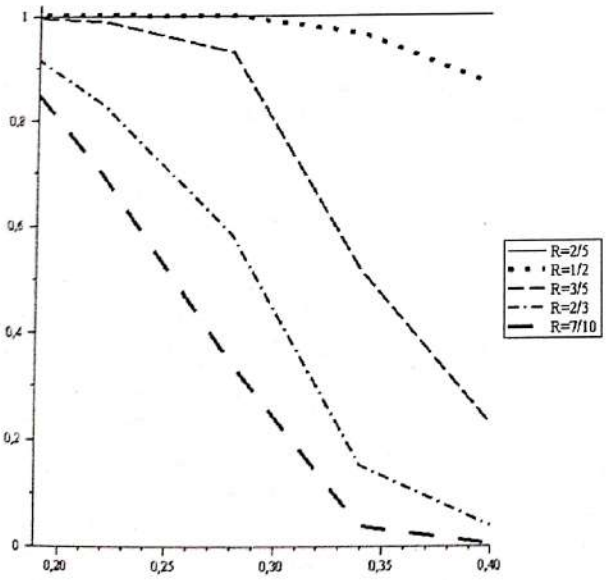

Fig. 5. Recovering capability (φ) of MDS block codes with differentrates in terms of the erasure probability of the channel

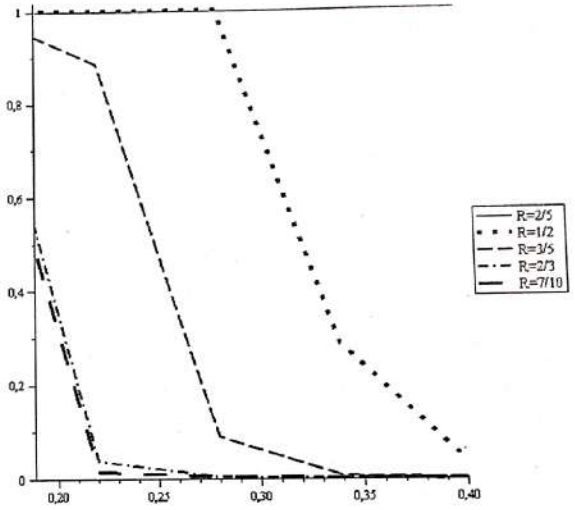

Fig.6. Recovering capability of reverse-MDP convolutional codes with different rates in terms of the erasure probability of the channel

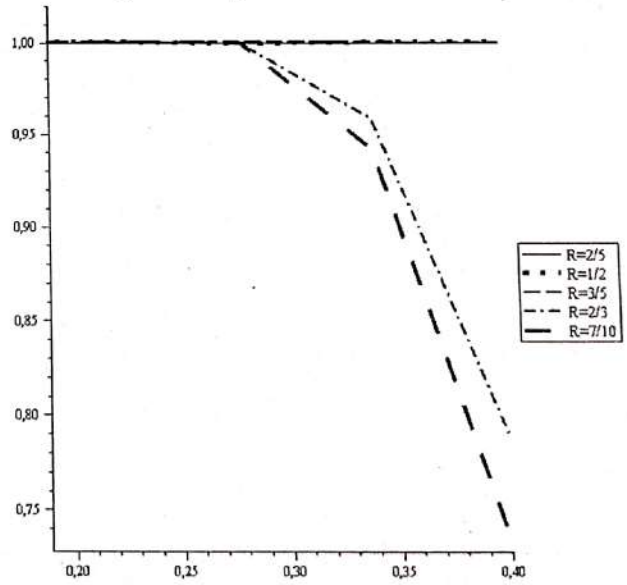

Fig.7Recovering capability of complete-MDP convolutional codes with different rates in terms of the erasure probability of the channel

Figure 5 reflects the behavior of MDS codes over the erasurechannel when choosing codes with different rates and overchannels with different erasure probabilities. The recoveringcapability is expressed in terms of φ = #erasures recovered /#erasures occurred .In Figures 6 and 7 we can see the performance of reveres-MDP and complete-MDP convolutional codes, respectively.The codes were chosen to have equal transmission rate andrecovering rate per window to those of the MDS block codesused in the simulations of Figure 5.The new simulation for reverse-MDP convolutional codes hows that reverse-MDP codes only outperform MDS codesat low rates. If we compare Figures 6 and 5, one can see thatonly for rates equal to R = 2/5 and R = 1/2 the results arebetter using reverse-MDP convolutional codes.

However, observing the results in Figure 7, one can seehow complete-MDP convolutional codes give much betterperformance than MDS block codes. Even though the rate decreasesfor convolutional codes when we increase the erasureprobability, the behavior is better than in the MDS case.

VI. COMPARISON BETWEEN MDS BLOCK CODES AND MDPCONVOLUTIONAL CODES

As we have already pointed out through several examplesMDP convolutional codes often are capable of decoding moreerasures than comparable MDS block codes. In this sectionwe would like to give some theoretical results on the decodingcapabilities of (complete) MDP convolutional codes andcompare these codes with MDS block codes of the same rate.

As a first goal we will show that a rate k/n convolutionalcode will not be able to decode erasures at a rate of more than(n-k)/=n. The following theorem serves this purpose.

VII. CONCLUSIONS

In this paper, we have discuss a comparison of LDPC block and convolutional codes based on several channels which shows some complexity, including computational complexity, hardware complexity, memory requirements, decoding delay, and BER/FER performance.. It has been shown via computer simulations that LDPC convolutional codes have an error performance comparable to that of their block code counterparts. In addition, several interesting tradeoffs have been identified between the two different types of codes with respect to VLSI implementation.

For erasure channels, while close-to-optimal performance(in the sense of approaching capacity) was achievable for theBEC, we showed that the structure of LDPC-CC imposed constraintsthat bounded the performance over erasure channelswith memory strictly away from the optimal performance (inthe sense of approaching MDS performance). Nevertheless, thesimple structure and good performance of these codes, as wellas the latency flexibility and low complexity of the decodingalgorithm, are attractive characteristics for practical systems.

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Hexagonal Multiband Patch Antenna for 4G Technology

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Abstract: **A new high gain, multiband hexagonal-shape slot loaded microstrip patch antenna is presented in this paper. The antenna is printed on a dielectric substrate, backed by a metal board, and directly fed from a 50 Ω coaxial cable. Using IE3D software package of Zeland, according to the set size, the antenna is simulated. The introduction of rectangular slot in hexagonal antenna offers a low profile, multiband, high gain and compact antenna. The computer simulation results show that the antenna can realize multiband characters at resonant frequencies of 7.4 GHz, 8.51 GHz and 9.8 GHz as in 4G technology.**

I. INTRODUCTION

In this paper a printed multiband antenna fed by a coaxial probe is presented. The antenna is simulated using IE3D, 14.10 version of Zealand. The results show the impedance bandwidth has achieved a good match. Besides to make sure that the antenna designed in this paper can be applied into practice for 4 G technology like virtual navigation, tele-medicine and multimedia transmission. The technology is commercially available from 2010 and already in use. An antenna with multiband nature can cater to different applications via a single antenna with low cost.

II. ANTENNA DESIGN

The geometry of the proposed hexagonal shaped slot antenna is shown in Figure 1. The antenna is built on a glass epoxy substrate with dielectric constant 4.4 and height h of 1.578 mm. A substrate of low dielectric constant is selected to obtain a compact radiating structure. The geometry of the top view of the proposed antenna is shown in Figure 1. The dimensions of the slotted patch are shown. Reducing the size of the antenna and multiband characteristic are one of the key factors for communication devices. Coaxial probe feed is used for multiband characteristic.

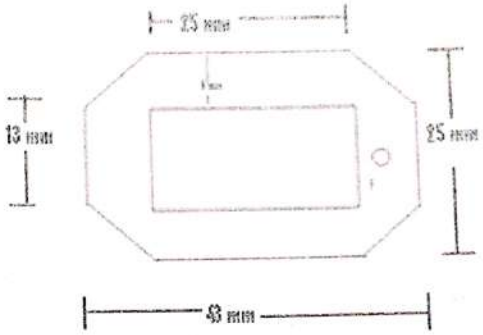

Fig.1 Geometry of the proposed hexagonal microstrip antenna

TABLE I. Dimensions of the hexagonal microstrip patch antenna

Dimension	Value
Length of rectangular patch	43 mm
Width of rectangular patch	25 mm
Feed point	(18,0)
Permittivity of dielectric	4.4
Loss tangent	0.02
Height of dielectric	1.578 mm
Effective dielectric constant	2.098

III. RESULT

The performance of this antenna was simulated and optimized by IE3D 14.10 version of Zeland. This was used to calculate the return loss and radiation pattern. The simulated return loss of the proposed antenna is shown in the Figure 2. The simulated result shows that the resonant frequency locates at about 7.4 GHz, 8.51 GHz and 9.8 GHz in the 4 G frequency spectrum. The simulated return loss graph and the 2-D radiation plot of the proposed antenna are shown in Figure 3.

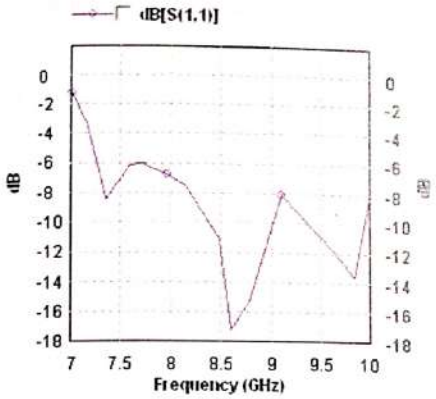

Fig.2 Simulated return loss for the hexagonal microstrip patch antenna

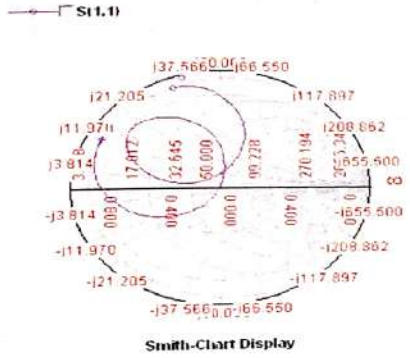

Fig.3 Simulated 2-D radiation plot

IV. CONCLUSIONS

A novel compact, slot loaded hexagonal microstrip antenna for multiband application for 4G has been designed, simulated and analyzed theoretically. Simulation results of a multiband microstrip patch with resonant frequencies at 7.4 GHz, 8.51 GHz and 9.8 GHz. have been present. Antenna performance can be enhanced by adjusting the probe position and the dimensions of the patch. It can be concluded that the proposed antenna has satisfactory multiband performance in the 4G spectrum.

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My sincere thanks to Amity University, Noida for the preparation of the paper and support of my fellows peers.

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A Robust Handoff Approach for 4G Cellular Networks using MATLAB

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***Abstract*-In Wireless Mobile Cellular Networks, users usually move between heterogeneous networks. In this type of environment, handoff procedure algorithm, handoff decision and its management is very important issue. Wireless Mobile Cellular Network supports the handoff process for users between various wireless technologies such as WLAN, CDMA and modern 3G networks. Heterogeneous networks are integrated in 4G wireless. To have seamless communication and mobility between these heterogeneous wireless access networks, support of vertical handoff (EVH) is required. Vertical handover is the convergence of heterogeneous networks for e.g.:- handover process between wireless cellular networks and WLAN. In this paper one of the handoff algorithms is discussed for different path loss models. Actually, the requirement to initiate handoff arises when the Received Signal Strength of the current base station falls below the threshold value. It adaptively controls the handoff according to the requirements of cells [13] and [14]. In this paper a simple and robust EVH algorithm for handoff procedure is discussed. The algorithm considers the parameters for all the networks under evaluation and then decides about the handoff by comparing the minimum threshold parameters with the values of current network as well as next all possible networks. This algorithm supports better service quality for all kind of networks with almost zero Call Blocking Probability.**

***Index Terms* -Cellular Network, Heterogeneous Network, Handoff, BS (Base Station), Received Signal Strength, Network Capacity, CDMA Networks and Call Blocking Probability.**

I. INTRODUCTION

In a cellular communication system, mobiles move in the service area and require communication services in the form of a wireless connection. In this system, total area is divided into smaller parts called cells to allow frequency reuse concept to increase the number of users in the network (Network Capacity). Large capacity with good service quality and minimum noise is always advantageous and also desirable.

[1] Frequencies used in one wireless service cell of the cluster can be reused in other distant cells. Every cell is controlled by its own transmitter and receiver to serve the mobile customers within its range. Calls can be handed off from one cell to another cell to maintain good quality phone service as the mobile moves between cells. A group of mobile customers having mobiles with a large range of mobility can access around in the overall network generating heavy flow of mobile traffic [11] and [12]. When the traffic load is concentrated in a cell, this cell becomes the hotspot cell. Therefore, the need arises for a proper traffic driven handoff management scheme [2]-[4]; so that mobile users will automatically move from congested cell to allow the network to balance itself dynamically in this situation.

II. HETEROGENEOUS NETWORK

These Heterogeneous Networks [4], [12] and [17] are the network used to connect computers and other devices with different operating systems and/or protocols. Example: A LAN connecting Microsoft Windows and Linux based PCs with Apple Macintosh Computers forms a heterogeneous network.

It also incorporates different technologies. Example: A wireless network which provides a service through a wireless LAN. This is able to provide and continue the service, when switching to a mobile network. This N/W is called, "**Heterogeneous Network**".

III. HANDOFF

In a wireless mobile cellular network handoff is the transition for any given user of signal transmission from one BS to an adjacent BS as the mobile user moves around [1]. In ideal cellular telephone network, each end user's mobile or modem (hardware of the subscriber) is always within the range of a BS. The area covered by each BS is called "Cell" [1]. The size and shape of cell depends upon the nature of the terrain. The cells in the network can overlap. For some time the hardware of subscriber may be in the range of two cells. The network decides which BS to handle the signal from the subscriber. Each time a mobile passes from one cell to another, the network automatically switches the responsibility of coverage from one BS to other. It is called, "**Hand OFF**" [8].

IV. PURPOSE

- To provide reliable wireless connectivity during the movement of mobiles between two cells.
- In non CDMA communication networks when the channel used by the mobile customer becomes interfered by other mobile user using the same channel in some other cell, the call is transferred to a different channel in the same cell or to a different channel in another cell in order to avoid the interference [1] [16] .
- Again in non CDMA networks, when the behavior of user changes. Example: Traffic based, when a fast traveling user connected to a large umbrella cell stops, then the call may be transferred to a smaller macro cell or even to a microcell in order to free capacity on the umbrella cell for other fast travelling users. Additional purpose of handoff is also to decrease the possible interference with other cells or users. This works in reverse also [1][15] and [16].
- When the capacity of connecting new calls for the given cell is used up. An ongoing call located in an area overlapped by some other cell is transferred to that cell to free some capacities [4].
- In CDMA networks a soft handoff may be induced in order to reduce the interference to a smaller neighboring cell due to the "**Near Far Effect**", even when the mobile customer still has an excellent connection in its current cell [1].
- When a user is detected moving faster than a particular threshold, the cellular call can be transferred to a larger umbrella cell in order to reduce the frequency of the handovers due to the movement [1].

V. HARD HANDOFF

Hard Handoff [6], [9] and [10] is the process in which the channel in the current cell is released and only then the channel in the new cell is engaged. Thus the connection to the current cell is broken before the connection to the new cell is made. That's why these handovers are called as, "**Break before Make**". Hard handovers are intended to be instantaneous in order to minimize the disruption to the call / to reduce the possibility of ending of call / Call Blocking Probability. A hard handover is perceived by

communication network engineers as an event during the call.

VI. SOFT HANDOFF

Soft Handoff [6], [9] and [10] is the process in which the channel of current cell is retained. It is used for some time in parallel with the channel in the new target cell. In this case the connection to the new target cell is established before the connection to the source cell (previous) is broken. So, this type of handoff is also called, "**Make before Break**". This time duration, during which both two channels are used in parallel, will be very brief. Due to this reason the soft handover is perceived by the communication network engineers as a state of call, rather than a brief event. Soft handover involves use of channels / connections of more than two cells. Example: Three, four or more cells can be maintained by one phone at the same time. When the call is in the state of soft handoffs, the signal of the best of all used channels can be used for the call at a given instant of time or all the signals can be combined to generate a clear copy of the signal.

The later is better choice. When such combinations are used, both in the down link and up link, the handover process is known as "Softer". Softer calls can be possible only when the cells involved in the handovers have a single cell site [15] and [16].

VII. HANDOFF IMPLEMENTATION

For realization of handoffs in a wireless cellular network practically, each cell is assigned with a list of potential new target cells. These cells can be used to hand over calls from the original source cells to them. These assigned target potential cells are called as "Neighbors" and the list is called "Neighbor List". Creation of these lists requires special computer tools. They are used to implement different algorithms. They may use input data obtained from field measurements or computer predictions of radio wave propagation in the regions covered by the cells [1], [8].

During a mobile call one or more parameters of the signal in the channel in the original source cell are monitored and assessed in order to decide when a handover is required. The handover may be requested by the user mobile or BTS of the current source cell. In some systems handover may be requested by the BTS of the neighbouring cell. The mobile user and the BTSs of the neighbouring cells monitor signals of each other. The best candidates are selected among the neighbouring cells. In CDMA, a target candidate may be selected among the cells which are not in the list of neighbour. This is done to reduce the probability of interference due to near far effect [15] [17] and [18].

VIII. MEASUREMENT AND PROCEDURE FOR A SIMPLE AND ROBUST VH ALGORITHM

Procedure of Handoff can be divided into three phases: measurement, decision and execution as illustrated in Figure 1. In the handoff measurement phase, the required information needed to make the handoff is calculated/ measured. Typical downlink measurements performed by the mobile are the E_c/ I_0 of the Common Pilot Channel (CPICH) of its current serving cell and surrounding cells. For certain types of handoff, other measurements are also required. In the decision phase of the handoff process, the calculated/ measured results are compared against the defined thresholds levels and then it is decided whether to start the

handoff process or not. All handoff algorithms have different triggering requirements/ conditions. In the execution phase, the handoff process is done and the relative parameters are changed according to the different types of this handoff process. As an example, in the execution phase of the CDMA handoff, the mobile enters or leaves the soft handoff state, a new BS is added or released, and the active set is updated [15], [16], [17] and [18].

[5], [12]. An adaptive RSS threshold is recommended to use so that the mobile user has enough time to initiate the handoff process. Therefore, the threshold value to initiate handoff should be carefully selected in order not to degrade QoS of other users. In this algorithm handoff time is controlled. It is called adaptive RSS threshold (Thresmin).Thresmin value avoids too early or too late initiation of the handoff process. Handover is completed before the mobile user moves out of the coverage area of the serving network of the cell.

In this simple and robust EVH algorithm the same procedure is followed. The discussed algorithm considers the parameters for all the networks under evaluation such as: Current Available Bandwidth, Received Signal Strength, Estimated Time MS will be in present network, Power Dissipation in Network, Mean number of request arrivals per unit time, Mean number of calls serviced per unit time, Power Consumption and Network Conditions etc. then decides about the handoff by comparing the minimum threshold parameters such as Threshold Current Available Bandwidth, Threshold Received Signal Strength and Threshold Estimated Time MS will be in present network etc. with the values of current network as well as next all possible networks with almost zero Call Blocking Probability.

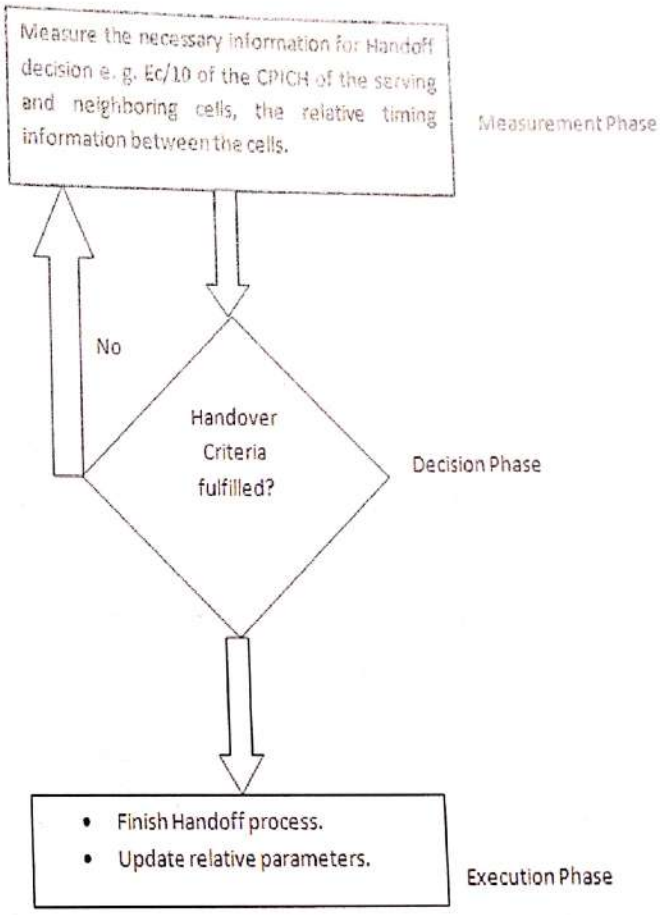

Figure 1. Handoff Procedure

IX. SIMULATION RESULTS

The simulations are performed in MATLAB, the assumptions made are:

(i) Wireless Radio model:Hata Okumura path loss model, Normal shadowing log spiral model and Free space path loss models etc.

(ii) Radius of cell: 1 km

(iii) Carrier Frequency 500 MHz to 1000 MHz

(iv) Antenna Heights 30m to 200 m.

(v) Mobile Station Height 1 m to 10m.

(vi) Distance between BS and MS 1km to 20 km.

Simulation is done for the following parameters in two example cases:

PARAMETERS USED & RESULT FOR CASE 1:

PARAMETERS:

The number of networks under evaluation N: = 2

Now enter the threshold values of all parameters when prompted:

Threshold Current Available Bandwidth: 30

Threshold Received Signal Strength: 40

Threshold Probable Time MS will be in present network: 10

Enter the values for the N/W 1 when prompted:

Enter the parameter values in currently connected network:

Current Available Bandwidth: 40

Received Signal Strength: 50

Probable Time MS will be in present network: 15

Power Dissipation in Network: 45

Mean number of service request arrivals in unit time: 15

Mean number of mobile calls serviced per unit time: 13

Enter the N/W Dependent Weights to the following:

Power Consumption: 10

Network Conditions: 15

Enter the values for the N/W 2 when prompted:

Current Available Bandwidth: 20

Received Signal Strength: 30

Probable Time MS will be in present network: 7

Power Dissipation in Network: 35

Mean number of service request arrivals in unit time: 30

Mean number of mobile calls serviced per unit time: 19

Enter the N/W Dependent Weights to the following:

Power Consumption: 10

Network Conditions: 15

RESULT:

No other network is having minimum service quality better than threshold. Stay in same network i.e. No handoff for these two networks under evaluation with above parameters. MATLAB result is shown in Figure 2.

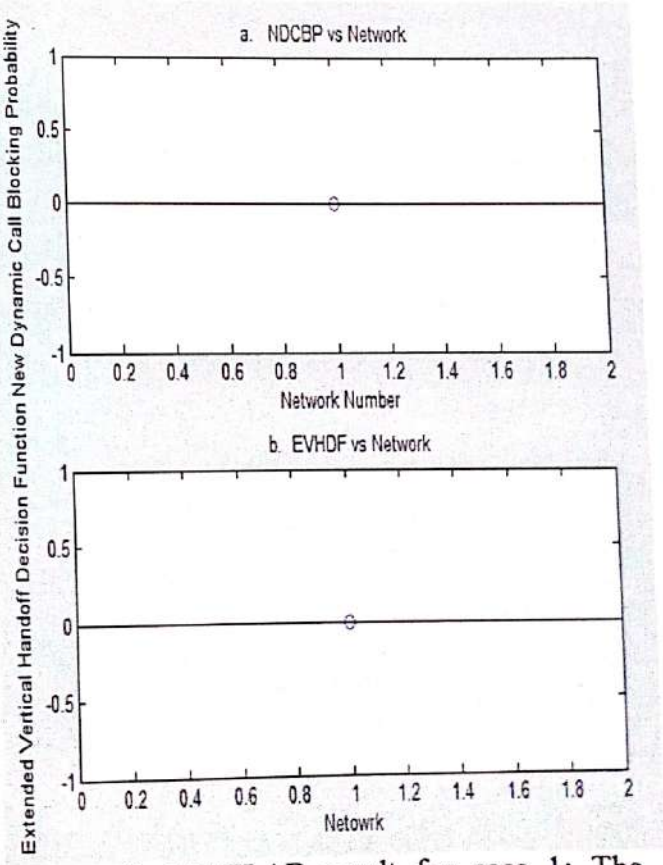

Figure 2. MATLAB result for case 1: The

graphs for New Dynamic Call Blocking Probability and Vertical Handoff Decision Function Vs Network.

PARAMETERS USED & RESULT FOR CASE 2:

PARAMETERS:

The number of networks under evaluation N: = 2

Enter the threshold values of all parameters when prompted:

Threshold Current Available Bandwidth: 30

Threshold Received Signal Strength: 40

Threshold Probable Time MS will be in present network: 10

Enter the values for the N/W 1 when prompted.

Enter the parameter values in the currently connected network:

Current Available Bandwidth: 22

Received Signal Strength: 25

Probable Time MS will be in present network: 15

Power Dissipation in Network: 15

Mean number of service request arrivals in unit time: 20

Mean number of mobile calls serviced per unit time: 15

Enter the N/W Dependent Weights to the following:

Power Consumption: 20

Network Conditions: 15

Enter the values for the network number 2 when prompted:

Current Available Bandwidth: 42

Received Signal Strength: 45

Probable Time MS will be in present network: 14

Power Dissipation in Network: 12

Mean number of service request arrivals in unit time: 20

Mean number of calls serviced per unit time: 18

Enter the N/W Dependent Weights to the following:

Power Consumption: 18

Network Conditions: 15

RESULT:

Handoff to new network with Network ID 2 i.e. Handoff is required and now the mobile should move to network 2 for these two networks under evaluation with above parameters. MATLAB result is shown in Figure 3.

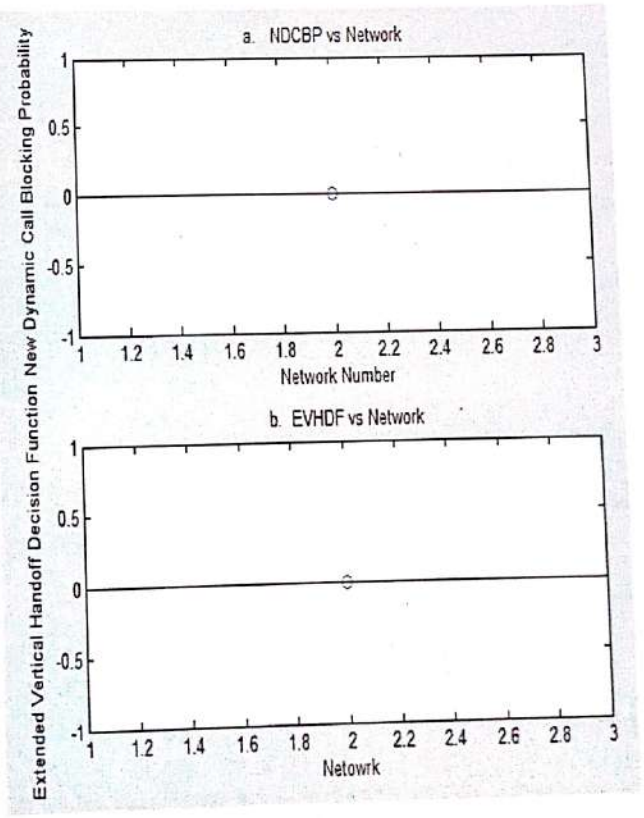

Figure 3. MATLAB result for case 2: The graphs for New Dynamic Call Blocking

Probability and Vertical Handoff Decision Function Vs Network.

CONCLUSION

A vertical handoff management algorithm scheme is presented in this paper for heterogeneous wireless cellular networks. The Dynamic Call Blocking Probability and Vertical Handoff Decision Function have been studied for all networks under evaluation with the decided parameters of algorithm have been simulated in the MATLAB. During simulation this algorithm evaluates all the networks with all possible handoff steps with the decided parameters and takes the decision regarding handoff based on the values of network available for the particular network. Here we simulated the results for Call Blocking Probability and Handoff Decision Function, results show that in case 2, handoff will occur in network 2 and handoff is not required for case 1. In case 2, handoff occurs in network ID 2 with zero call blocking probability. The algorithms is good for cases of handoff between WLAN and advanced and fast networks such as 3G as it decides handoff with zero call blocking probability and evaluates the network for a large number of parameters before making handoff decision so this algorithm also avoids the unnecessary handoffs. In future this algorithm can be compared with other algorithms with decides for handoff adaptively by considering other parameters such traffic load, RSS, hysteresis and fading conditions etc.

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Throughput based handover in a Wi-Fi network

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Abstract—**As the technology is improving so are the demands of end users and their applications increasing. A wide variety of new applications are being invented daily. These applications have different demands from the underlying network protocol suite. Several issues need to be taken into account while considering a wireless network. Quality of service (QoS) is one of the most important among all.In this paper we have purposed a handover mechanism for IEEE 802.11 to study the QoS in terms of throughput. The objective of the paper is to study the variations in average throughput with several factors like speed of the moving node, packet size, interval etc. with the help of Network Simulator Version 2 (NS-2) software.**

Keywords— **Homogeneous network, QoS (Quality of service), IEEE 802.11, Wi-Fi, Network simulator version 2.**

I. INTRODUCTION

Wireless networking is an emerging technology now adays. Support for mobility in Internet access is gaining significant interest as wireless/mobile communications and networking are proliferating, especially boosted by the widespread use of laptops and handheld devices. Now when a mobile node is moving, it can roam around a single network means from the range of one base station to another. Also it can move from one network to another network. This process in technical terms is known as handoff.

When the mobile node switches between base stations or access points within the same wireless networks is called horizontal handoff and the network environment is known as homogeneous network. When it switches between heterogeneous networks is called vertical handoff. Viz., the handoff within Wi-Fi is known as horizontal handoff and the handoff from Wi-Fi to WiMAX is known as vertical handoff. When a mobile node undergoes a handoff, a major issue that needs to be considered is the QoS (Quality of service). Quality of service is the ability to provide different priority to different applications, users, or data flows, or to guarantee a certain level of performance to a data flow. QoS in wireless networks is usually managed at the MAC layer.QoS in an application depends mainly on the following factors:

1) End to End delay
2) Jitter
3) Throughput
4) Packet loss

For the simulation purpose, in this paper we are using the NS 2 (Network simulator version 2) software. The focus of this paper is basically on throughput. The objective is to derive the variations of throughput with a number of parameters like speed of the node when it moves from one base station to another base station in a Wi-Fi network environment, the packet size of data to be transferred, interval etc.

Beyond local area network, the first technology which comes into existence for wireless networking is Wi-Fi. WLAN is based on short-range RF communications, standardized in the USA by one of the Institute of Electrical and Electronics Engineers (IEEE) working groups.

II. OVERVIEW OF THE TECHNOLOGY

As wireless networking grows in popularity, various radio access technologies have been developed to provide better environment for user data service. Most of all, IEEE 802.11 Wireless Local Area Network (WLAN) is one of the dominant wireless technologies to support high-speed network access nowadays. The WLAN basically forms an infrastructure with two network components, Access Point (AP) and Station (STA). An AP is generally distributed at a fixed location, and the WLAN infrastructure connects STAs to a wired network via the AP within their communication range. AP's signal range is denoted by Basic Service Set (BSS) or hotspot which generally provides coverage within a few ten-meter radius.

Wi-Fiis trademark of the Wi-FiAlliance. The technical term "IEEE 802.11" has been used interchangeably with Wi-Fi, however Wi-Fi has become a superset of IEEE 802.11 over the past few years. The 802.11 family includes over-the-air modulation techniques that use the same basic protocol. The most popular are those defined by the 802.11b and 802.11g protocols, which are amendments to the original standard. 802.11-1997 was the first wireless networking standard, but 802.11b was the first widely accepted one, followed by 802.11g and 802.11n. Security was originally purposefully weak due to export requirements of some governments and was later enhanced via the 802.11i amendment after governmental and legislative changes. 802.11n is a new multi-streaming modulation technique. Other standards in the family are service amendments and extensions or corrections to the previous specifications.

The IEEE 802.11 standard provides low cost and effective wireless LAN service. The deployment of high speed network (11Mbps in 802.11b and 54Mbps in 802.11a/g) can be easily established by the free and unlicensed spectrum (2.4GHz in 802.11b/g and 5GHz in 802.11b). The IEEE 802.11b standard

is one of the most commonly used standards for the WLAN. There are 11 available channels in this standard and 3 of them are non-overlapping channels. On the PHY layer, it employs the Direct Sequence Spread spectrum (DSSS) technique with Complementary Code Keying (CCK) modulation scheme. This standard operates in two modes: one is Ad Hoc mode and the other is Infrastructure mode.

The Ad Hoc mode of operation allows the computing devices within range of each other to discover and communicate in peer to peer fashion without involving central access points. In an infrastructure type of a WLAN, an Access Point is used to connect computing devices to connect wired nodes.

III. HANDOFF

In cellular telecommunications, the term handover or handoff refers to the process of transferring an ongoing call or data session from one channel connected to the core network to another.The most basic form of handover is when a phone call in progress is redirected from its current cell(called source) and its used channel in that cell to a new cell (called target) and a new channel. In terrestrial networks the source and the target cells may be served from two different cell sites or from one and the same cell site (in the latter case the two cells are usually referred to as two *sectors* on that cell site). Such a handover, in which the source and the target are different cells (even if they are on the same cell site) is called inter-cell or vertical handover. The purpose of inter-cell handover is to maintain the call as the subscriber is moving out of the area covered by the source cell and entering the area of the target cell.

A special case is possible, in which the source and the target are one and the same cell and only the used channel is changed during the handover. Such a handover, in which the cell is not changed, is called intra-cell or horizontal handover. The purpose of intra-cell handover is to change one channel, which may be interfered, or fading with a new clearer or less fading channel. In this paper we have taken into account, a horizontal handover in a WLAN network.

IV. THROUGHPUT

Network throughput is the average rate of successful message delivery over a communication channel. This data may be delivered over a physical or logical link, or pass through a certain network node. The throughput is usually measured in bits per second (bit/s or bps), and sometimes in data packets per second or data packets per time slot. The system throughput or aggregate throughput is the sum of the data rates that are delivered to all terminals in a network. The maximum throughput is equals to the TCP window size divided by the round-trip time of communications data packets. The maximum throughput is calculated as:

$$\text{Throughput} = \frac{\text{RWIN}}{\text{RTT}}$$

where RWIN is the TCP Receive Window and RTT is the round-trip time for the path. The Max TCP Window size in the absence of TCP window scale option is 65,535 bytes.

V. SIMULATION ENVIRONMENT

In this paper we have make use of NS2 software for the simulation purpose. NS2 is an object oriented discrete-event simulator for networking research which maintains list of events and executes one event after another. Back end of the NS2 is C++ event scheduler and front end is oTCL. It provides substantial support to simulate a bunch of protocols like TCP, UDP, FTP, HTTP and DSR.

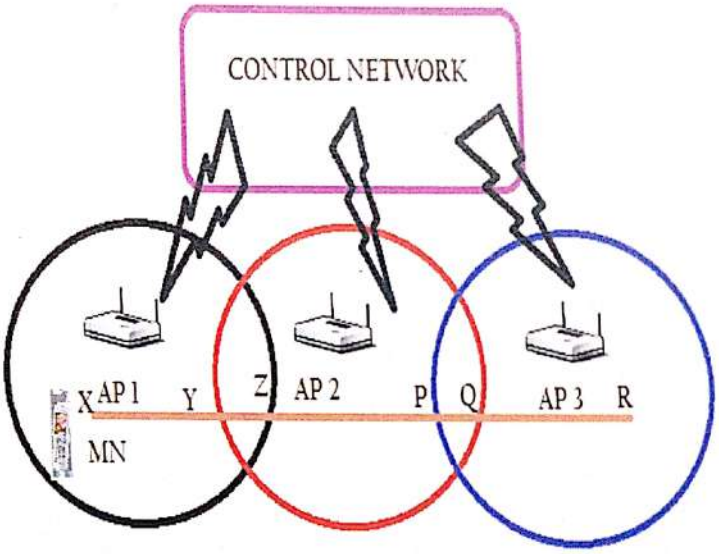

Fig.1. Network Scenario

In the considered network, we have taken a CN (Control network), a router, a mobile node and three base stations. AP1, AP2 and AP3 stands for access point 1, access point 2 and access point 3 respectively. Mobile node(MN) is moving from AP1 to AP2. X is any point inside the range of AP1, Y represents the outer range of AP2 and Z corresponds to maximumrange of AP1, P is the maximum range of AP3 and Q represents the outer range of AP2. Y-Z represents the overlapping region between AP1 and AP2 and P-Q represents the overlapping region between AP2 and AP3.

VI. RESULTS AND DISCUSSION

For the given scenario we have observed the following results upon varying the three parameters which are speed with which the mobile node moves from R2 to R4, packet size of the data and the interval of the CBR traffic source.

A. *Throughput with varying speed of mobile node*

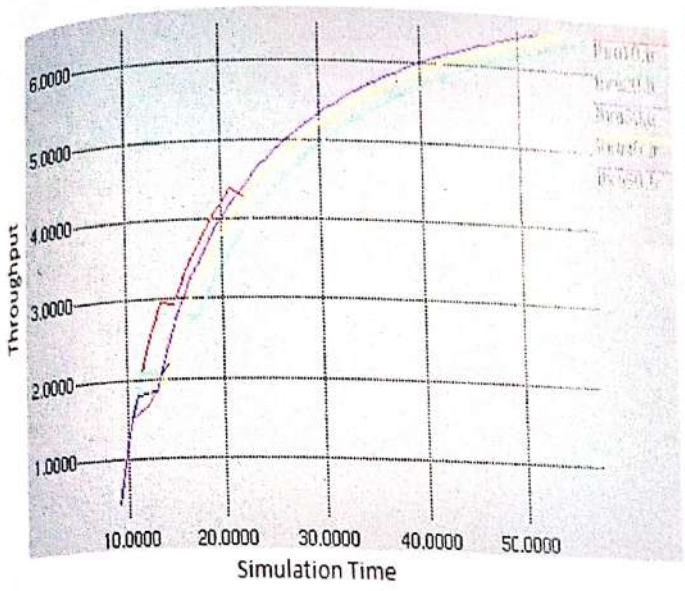

Fig.2. Throughput comparison for different speeds of mobile node

In above figure thru10.tr represents throughput corresponding to 10m/s speed of mobile node, similarly thru20.tr, thru30.tr, thru40.tr and thru50.tr represents throughput corresponding to 20m/s, 30m/s, 40m/s and 50m/s speed of the mobile node. Figure 2 represents the variations of throughput in a Wi-Fi network environment. From the figure we analyis that as the speed of the mobile node is increasing the throughput isdecreasing. The slight consistency in graph represents the handoff from one base station to another.

B. *Throughput with increased packet size*

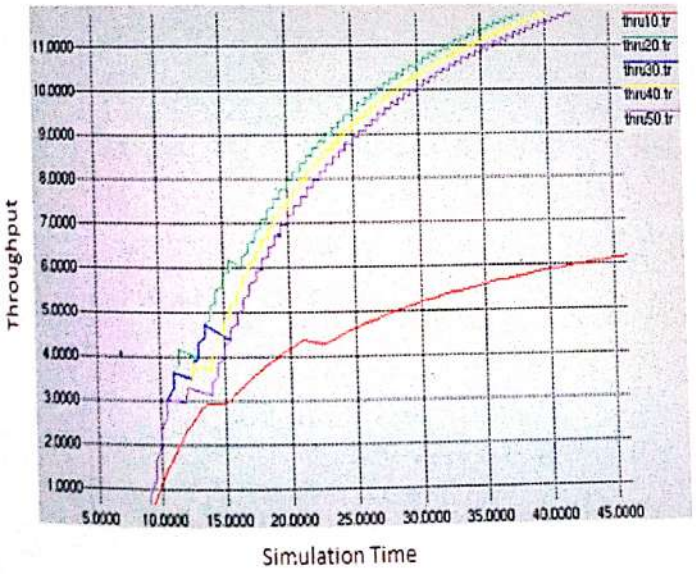

Fig.3. Throughput comparison for different speeds of mobile node with increased packet size

In above figure thru10.tr represents throughput corresponding to 10m/s speed of mobile node, similarly thru20.tr, thru30.tr, thru40.tr and thru50.tr represents throughput corresponding to 20m/s, 30m/s, 40m/s and 50m/s speed of the mobile node. Fig.3. represents the variations of throughput for different speeds of mobile node but also with increased packet size of the CBR traffic source which provides the data to be transferred. Initially packet size has been considered to be 500. But in the present case it is increased to 2000. In this figure we observed that with increased packet size upon increasing speed of the mobile node, throughput is also increased slightly.

C. *Throughput with decreased interval*

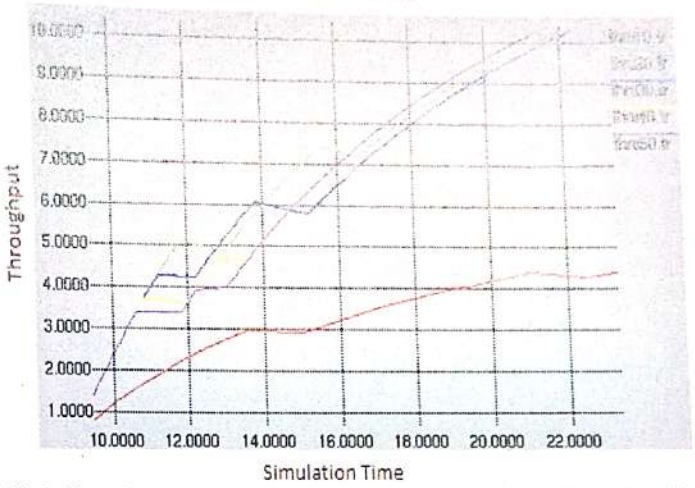

Fig.4 Throughput comparison for different speeds of mobile node with decreased interval

Once again thru10.tr in the figure represents throughput corresponding to 10m/s speed of mobile node, similarly thru20.tr, thru30.tr, thru40.tr and thru50.tr represents throughput corresponding to 20m/s, 30m/s, 40m/s and 50m/s speed of the mobile node. Fig.4 represents the variations of throughput for different speeds of mobile node but with decreased interval of the CBR traffic source. In the 1st case interval value was 0.5. Now it is reduced to 0.2 and result is a slight increase in throughput.

D. *Throughput with increased packet size and decreased interval*

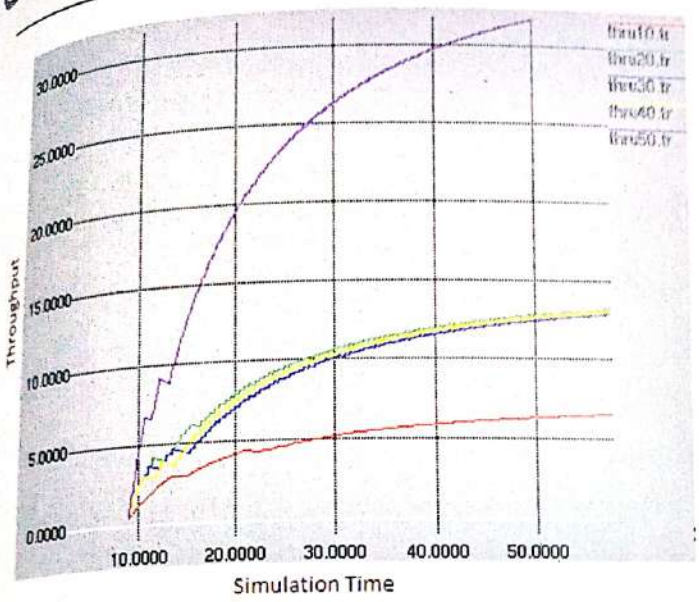

Fig.5 Throughput comparison for different speeds of mobile node with increased packet size and decreased interval

In above figure thru10.tr represents throughput corresponding to 10m/s speed of mobile node, similarly thru20.tr, thru30.tr, thru40.tr and thru50.tr represents throughput corresponding to 20m/s, 30m/s, 40m/s and 50m/s speed of the mobile node. Fig.5 represents the variations of throughput for different speeds of mobile node also with increased packet size and decreased interval. Throughput is again increased slightly.

VII. CONCLUSION

In this paper we have studied the performance characteristics of a Wi-Fi network in terms of throughput variations using NS2. Frequent handovers for a short time period mean a higher chance of adversely affecting the overall throughput. But as a result of this paper we have concluded that if the speed of the mobile node is increasing, if we use a greater packet size and a small interval for the CBR traffic source, we can achieve an increase in throughput

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A New Wireless Communication Technology: Radio over Fiber

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Abstract: Radio over Fiber is an upcoming wireless standard which is being designed to seamlessly integrate many different standards as well as integrate broadband communication wirelessly. This paper will give a brief overview of the beginnings of wireless technology and how it has evolved to what it has become today. This paper will discuss features of Radio over Fiber operating at Millimeter Frequency Spectrum wireless communication technique. Also provide comparison with existing mobile communication techniques up to fourth Generation.

1. Introduction

For the future provision of broadband, interactive and multimedia services over wireless media, current trends in cellular networks, both mobile and fixed are to reduce cell size to accommodate more users and to operate in the microwave/millimeter wave frequency to avoid spectral congestion in lower frequency bands and the radio frequency bands for wireless communication systems are shown in Table 1.1. Thus, it demands a large number of base stations to cover a service area and cost-effective BS is a key to success in the market. This requirement has led to the development of system architecture where functions such as signal routing/processing, handover and frequency allocation are carried out at a central CS, rather than at the BS.

Table 1.1 Radio Frequency Bands for Wireless Communication Systems

Band No.	Frequency Subdivision	Frequency Range	Wavelength
4	VLF (very low frequency)	Below 30kHz	Greater than 10 km
5	LF (low frequency)	30 to 300kHz	10km to 1km
6	MF(medium frequency)	300 to 3000kHz	1km to 100m
7	HF(high frequency)	3 to 30MHz	100m to 10m
8	VHF(very high frequency)	30 to 300MHz	10m to 1m
9	UHF(ultra high frequency)	300 to 3000MHz	1m to 10cm
10	SHF(super high frequency)	3 to 30GHz	10cm to 1cm
11	EHF(extremely high frequency)	30 to 300GHz	1cm to 1mm

Furthermore, such a centralized configuration allows sensitive equipment to be located in safer environment and enables the cost of expensive components to be shared among several BSs. An attractive alternative for linking a CS with BSs in such a radio network is via an optical fiber network, since optical fiber has low loss, is immune to EMI and has broad bandwidth [1]-[5]. Wireless broadband technologies promise to make all kinds of information available anywhere, anytime, at a low cost to a large portion of the population. New wireless subscribers are signing up with an increasing demand of more capacity for ultra-high data rate transfer at speeds of 1Gbps and up, while the radio spectrum is limited. This requirement of more bandwidth allocation places heavy burden on the current operating radio spectrum. Radio over technology (RoF) has been proposed to over these problems [4]-[10]

2. Comparison Evolution between existing Mobile Communication Techniques

The purpose of this section is to give an overview of the evolution of wireless technology from the first generation (1G) to the fifth generation.

2.1. First generation wireless (1G)

First generation wireless technologies were designed to transmit voice wirelessly in the 1980s. Network signals were analogue and used Frequency Division Multiple Access (FDMA) to carry voice channels and could not support sending data from one point to another. This first generation of wireless communication was very unreliable, and not many users could use their cell phones at one time. It consumed more bandwidth to avoid inter carrier interface. Disadvantage was crosstalk which caused problem on other frequency and also disrupt transmission.

2.2. Second generation wireless (2G)

Second generation technology was deployed in the 1990s and uses circuit-based digital technologies. 2G systems were created to increase the capacity over the analog system. It used time Division Multiple Access(TDMA) 2G also has facility of Circuit-Switched Data(CSD) which provided data transmission via Internet Protocol(IPV4) GPRS was introduced in 2000 but slow speed 56kbps to 115kbps (kilobit/sec). compared with first-generation systems, higher spectrum efficiency, better data services, and more advanced roaming were offered by 2G systems.

2.3. An Update to Second Generation (2.5G)

2.5G Deployed in 2003 which implemented High Speed Circuit Switched Domain (HSCSD) Data rate 236.8kbps to 384kbps by using EDGE (Enhanced Data Rate for GSM Evolution) .It is considered a stepping stone between 2G and 3G technologies [5]-10]. Faster data transmission is also possible, yet transmission of video is still very slow with 2.5G.

2.4. Third generation wireless (3G)

3G was introduced to help to solve the problem of global communication and lack of standardization. 3G allows simultaneous use of speech and data services at higher rates and better spectral efficiency. More diverse multimedia contents like mobile TV, audio-video conferencing, video on demand, fax services and other broadband applications for entertainment and business solutions. High speed internet surfing includes UMTS (Universal Mobile Telecommunication System) and WCDMA (Wideband Code Division Multiple Access) which offer speed up to 1.92Mbps [6]-[9].

2.5. Upgradation to 3G (3.5G)

3.5G Upgraded and enhanced with higher data speed and capacity. Down-link speed 3.6, 7.2 to 14Mbps which was made possible with HSDPA (High-Speed Down-link Packet Access. Further increase of speed 42 to 84Mbps was achieved with HSPA (High Speed Packet Access) It is also referred as 3G+,3G Turbo,3G EDGE [8]-[10].

2.6 Fourth Generation(4G)

Fourth Generation (4G) is the next generation of wireless networks that will replace third Generation (3G) networks. 4G is intended to provide high speed, high capacity, low cost per bit, IP based services for video, data and Voice (VoIP).4G is all about an integrated, global network that's based on an open system approach. Constitute of 4G has not been standarized yet. It is non-backward compatible with new higher frequencies bands [8]-[12].

3. Radio over Fiber Technology

Radio over Fiber (RoF) technology uses optical fiber links to distribute RF signals from a central station to multiple remote access units due to its ability to provide simple antenna front ends, increased capacity, and multi radio wireless access coverage. It involves modulating the radio frequency (RF) sub-carrier onto an optical carrier for distribution over a fiber network. RoF technique has been considered a cost-effective and reliable solution for the distribution of the future wireless access networks.

The transmission of radio signals over fiber, with simple optical to electrical conversion, followed by radiation at remote antennas, which are connected to a central CS, has been proposed as a method of minimizing costs. The reduction in cost can be brought about in two ways. Firstly, the remote BS or radio distribution point needs to perform only simple functions with small in size and low in cost. Secondly, the resources provided by the CS can be shared among many BSs. This technique of modulating the radio frequency sub carrier onto an optical carrier for distribution over a fiber network is known as RoF system. This approach is in Fig.1.1. To be specific, the RoF system typically comprises a central CS, where all switching, routing and frequency management functions are performed, and an optical fiber network, which interconnects a large number of functionally simple and compact BSs for wireless signal distribution.

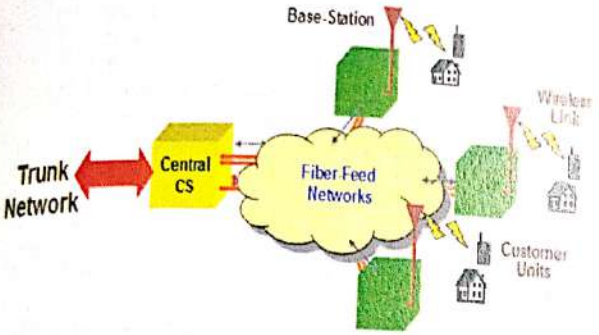

Fig. 1.1 Block diagram of the Fiber- Wireless Approach

The BS has no processing function and its main function is to convert optical signal to wireless one and vice versa. Since RoF system was first demonstrated for cordless or mobile telephone service, a lot of research efforts have been made to investigate its limitation and develop new, high performance RoF systems. Table 1.2 shows that RoF is needed for future broadband sevices.

4. Conclusion

In order to deploy next-generation mobile networks, there is a greater need for service portability and interoperability with the proliferation of mobile and portable digital devices, which requires devices to be connected seamlessly. The expansion of wireless ubiquity will drive an increased volume of consumers to access and rely on mobile networks creating a need for greater economies of scale and lower per bit cost. In response to this remarkable development, the metro and core networks of the telecommunication infrastructure have experienced a tremendous growth in bandwidth and capacity with the wide deployment of fiber optic technology in the past decade.

Table1.2 A Brief Comparison Evolution between RoF with existing Mobile Communication Techniques

Technology/ features	1G	2G/2.5G	3G	4G	RoF (Beyond 4G)
Deployment	1984	1999	2002	2010	2015
Data Bandwidth	2Kbps	14.4-64Kbps	2Mbps	200Mbps to 1Gbps	1Gbps and higher
Standards	AMPS	2G:TDMA,CDMA ,GSM 2.5G:GPRS, EDGE, 1xRTT	WCDMA, CDMA-2000	Single unified standard	Single unified standard
Multiplexing	FDMA	TDMA,CDMA	CDMA	CDMA	CDMA
Switching	Circuit based	Circuit based	Packet based	Circuit and packet switch	Packet Switch
Core Network	PSTN	PSTN	Packet Network	Internet	Internet

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Performance and Comparison of Wallace and Vedic Multiplier

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Abstract: Speed of the multiplier depends on the hardware and algorithm used for the multiplication. A high speed multiplier reduces the computational time and is an important hardware block in digital signal processing system. Vedic multiplier is different from conventional multiplier which uses adder and shifter. This paper compares 16X16 vedicmultiplier based on UrdhvaTiryakbhyam Sutra and 16X16 Wallace multiplication. The code for the above is simulated on ModelSim.Computation of LUT value is done on Xilinx 14.5.

Keywords: **Vedic multiplier, Wallace multiplier, Verilog, ModelSim, Xilinx**

I. INTRODUCTION

Multiplication is the process by which we multiply two numbers. A device which performs multiplication is called a multiplier. In terms of Digital Electronics a multiplier is a device which multiplies two binary numbers. Digital multiplier is the most common type of multiplier in any circuit design.Digital multipliers are important part of Digital Signal Processing Systems[1]. They are fast and reliable.They can be used to perform many operations and depending on the need of the circuit multiplier are selected.

Multipliers are extensively used in DSP applications such as convolution, FFT(Fast Fourier Transform) filtering and in microprocessors in their arithmetic and logic unit. They are also used in communication devices. In Signal and Image processing system the study and development of fast multiplier circuit has been taken up with keen interest.

Several steps of addition, subtraction and shift operations were used to implement multiplication operations. Most techniquesinvolve computing a set of partial products and then summing the partialproducts together [2]. There are various algorithm proposed which have trade off in speed,area and power consumption. Some of the multipliers are Booth multiplier, Wallace multiplier and Vedic multiplier.

Reducing power consumption and delay computation is very important requirement for many applications. Reduction in power consumption will lead to decrease in heat dissipation. Throughput and Latency are two important parametersfrom delay perspective.Throughput is the measure of how many multiplications can be performed in a given span of time.Latency on the other hand is the time required to calculate a function.

Vedic multiplier is afast and low power multiplier. A basic block of 2X2 multiplier is used as a sub block for 4X4 multiplier. A 4X4 block is used as a sub block for 8X8 multiplier and a 8X8 block is used as a sub block for 16X16 multiplier.

II. VEDIC MULTIPLIER

UrdhvaTiryakbhyam Sutra

"Vedic" originates from the word "Veda" which means a reservoir of knowledge. Vedic mathematics is a book written bySri BharatiKrsnaTirthaji[4]. The book published in 1965 describes calculation techniques based on vedas.
Vedic multiplication is divided into sixteen sutras[3]. This paper is based on the UrdhvaTiryakbhyam Sutra. The algorithm uses vertically and crosswise multiplication. As the partial products and their sum are calculated parallely the algorithm is independent of the clock frequency of the processor. Hence, it is well adapted to parallel processing. This in turn reduces delay, which is the primary aim behind this work. On comparing this algorithm to conventional multipliers this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly.This feature makes it more suitable for binary multiplications.

III. PROPOSED TECHNIQUE

A. 2X2 Vedic Multiplication

A 2X2 multiplier multiplies two numbers of 2bit each. Let the numbers be N(N_1 N_0) and M(M_1 M_0). Multiplication of the numbers is shown is equation 1.

$$\begin{array}{r} N_1\ N_0 \\ \times\ M_1\ M_0 \\ \hline N_1M_0\ \ N_0M_0 \\ N_1M_1\ \ N_0M_1 \\ \hline O_3\ \ O_2\ \ O_1\ \ O_0 \end{array} \qquad (1)$$

Figure 1: 2X2 multiplier

Firstly, the least significant bits of N and M are multiplied which gives the least significant bit of the final product O_0(vertical). Then, the LSB of the multiplicandis multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. Correspondingly sum becomes the third bit and carry becomes the fourth bit of the final product.The above module is known as 2X2 multiplier block.

B. 4X4 Vedic Multiplication

Now analyze a 4X4 Vedic block, say N_3N_2 N_1N_0 and $M_3M_2M_1M_0$. The output line for themultiplication result are $O_7O_6O_5O_4O_3O_2O_1O_0$.

Let's divide the number N and M into two parts, sayN_3 N_2 & N_1N_0 for N and M_3M_2 & M_1M_0 for M.Using fundamental of Vedic multiplication, takingtwo bits at a time and using 2 bit multiplier block we can have the following structure for multiplication as shown in equation 2.

$$\begin{array}{r} N_3N_2\ N_1N_0 \\ \times M_3M_2\ M_1M_0 \\ \hline \end{array} \qquad (2)$$

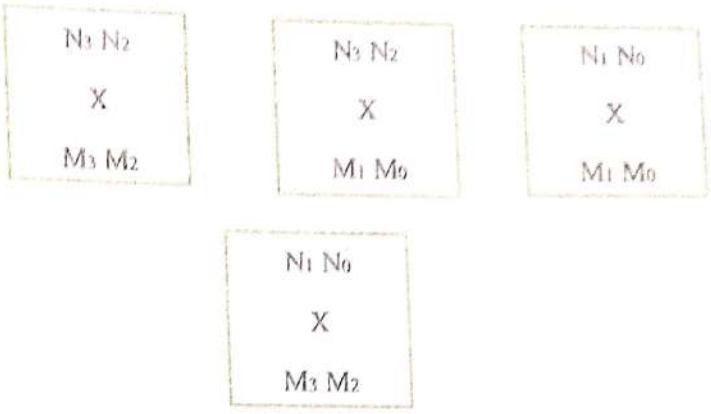

Figure 2: 4X4 multiplier

In figure 2 each block is a 2X2 bit Vedic multiplier. First 2X2 bit multiplier inputs are N_1N_0 and M_1M_0. The last block is 2X2 bit multiplier with inputs N_3 N_2 and M_3 M_2. The middle one shows two 2X2 bit multiplier with inputs N_3 N_2 & M_1M_0 and N_1N_0 & M_3 M_2. So the final result of multiplication, which is of 8 bit, O_7 $O_6O_5O_4$ O_3 O_2 O_1 O_0

C. 8X8 Vedic Multiplication

An example for 8X8 multiplication is given below. Let's say 8X8 bit multiplication of 11111111 and 00001001. We divide thenumber of bit equally and do the same analysis that used for 4X4 multiplications. It means, 11111111 will become 1111 and 1111. Similarly 00001001 will become 0000 and 1001. Hence the four different multiplications are shown in equation 3:-

$$\begin{array}{l} (1111x0000)\ (1111x1001)\ (1111x0000)\ (1111x1001) \\ \qquad\qquad 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\ \qquad\qquad X\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 1 \\ \qquad\qquad \text{---------- (3)} \\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \quad 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \quad 1\ 0\ 0\ 0\ 0\ 1\ 1\ 1 \\ \qquad\qquad 1\ 0\ 0\ 0\ 0\ 1\ 1\ 1 \\ \text{---------- (3)} \\ 0\ 0\ 0\ 0 \quad 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \quad 0\ 1\ 1\ 1 \\ \qquad\qquad 1\ 0\ 0\ 0\ 0\ 1\ 1\ 1 \\ \qquad\qquad 0\ 0\ 0\ 0\ 1\ 0\ 0\ 0 \end{array}$$

Figure 3: 8X8 multiplier

In figure 3 adder will add 00000000 and 10000111 giving sum as 10000111 with no carry out, and the adder will add the result of the adders with 00001000 and will result sum as 10001111. Since no carry is generated from either of the

adder, so adder will give both sum and carry out as zero, so nothing is to be added with 0000, so final result will be: O_0=1,O_1=1,O_2=1,O_3=0,O_4=1,O_5=1,O_6=1,O_7=1,O_8=0,O_9=0,O_{10}=0,O_{11}=1, O_{12}=0,O_{13}=0,O_{14}=0,O_{15}=0.The final answer happens to be 0000100011110111.

D. 16X16 Vedic Multiplier

The design of a 16X16 block is an optimized arrangement of 8X8 blocks. The first step in the design of 16X16 block is the grouping of 8 bit (byte) of each 16 bit input. These lower and upper bytes of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 8X8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are then added in a 16-bit carry look ahead adder optimally to generate final product bits. Block diagram is shown in figure 4.

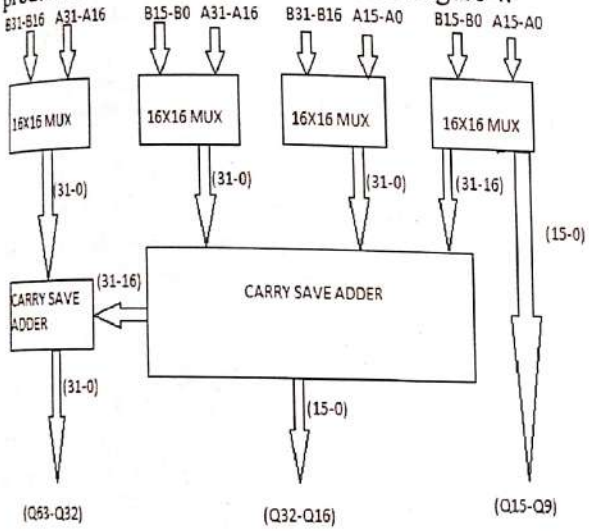

Figure 4: 16X16 multiplier

IV. WALLACE MULTIPLIER

Wallace tree is an efficient hardware algorithm that multiplies two integers, devised by Australian scientist Chris Wallace in 1964.Wallace multiplier is an efficient multiplier. Partial product array of N^2 bits are formed in the first step.In the second step, group of three rows is reduced by three 1 bit Full adders. Half adders are used for reducing two bits in a column. A single bit in a column is passed to the next stage in the same column without processing. This reduction procedure is repeated in each successive stage until only two rows are left [5]. In the final step, the remaining two rows are added using a carry propagating adder.

V. RESULT AND CONCLUSION

A. Vedic Multiplier

The output ofVedic multiplier is shown in figure 5 and figure 6.It accepts two number of 16 bits each and the result is a 32 bit number.

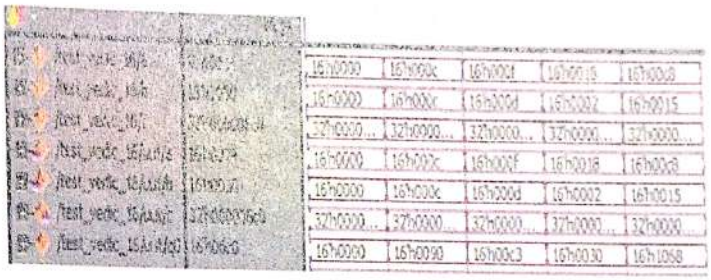

Figure 5:Output of Vedic Multiplier

16'h0000	16'h000c	16'h000f	16'h0018	16'h00c8
16'h0000	16'h000c	16'h000d	16'h0002	16'h0015
32'h0000...	32'h0000...	32'h0000...	32'h0000...	32'h0000...
16'h0000	16'h000c	16'h000f	16'h0018	16'h00c8
16'h0000	16'h000c	16'h000d	16'h0002	16'h0015
32'h0000...	32'h0000...	32'h0000...	32'h0000...	32'h0000...
16'h0000	16'h0090	16'h00c3	16'h0030	16'h1068

Figure 6: Outpur of Vedic Multiplier

Table I shows the number of sliced LUT used by vedic multiplier.

TABLE I :DEVICE UTILIZATION SUMMARY

Number of Slice LUTs	476	5,720	8%
Number used as logic	476	5,720	8%

B. Wallace multiplier

Output for Wallace multiplier is shown in figure 7.

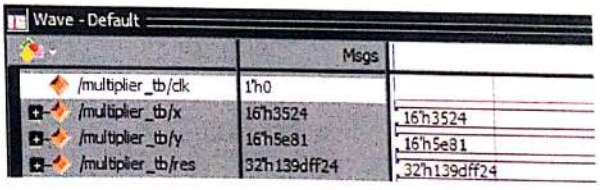

Figure 7: Output of wallace multiplier

Table II shows the number of sliced LUT used by Wallace multiplier

TABLE II : DEVICE UTILIZATION SUMMARY

Number of Slice LUTs	495	5,720	8%
Number used as logic	494	5,720	8%

Table III shows the LUT (lookup table) values for both Vedic and Wallace multiplier. The Verilog code is implemented on Spartan6E kit. The code is synthesized on Xilinx 14.5. The multiplier with more LUT value will require more transistor to run as shown in table III.

TABLE III
LUT VALUE OF VEDIC AND WALLACE MULTIPLIERS

Multiplier	LUT VALUE	KIT
Vedic	476	Spartan6E
Wallace	495	Spartan6E

Although both multiplier use 8% LUT value. Vedic multiplier has less LUT value then Wallace multiplier.

Comparing the LUT value of both the multiplier we find that Vedic multiplier will require less number of logic gates on a Spartan 6E kit.Fewer logic gates means less power is dissipated. Hence power consumption is less in Vedic multiplier.

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