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Comparative Analysis of CMOS based Pseudo Differential Amplifiers

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Abstract : *This paper presents a comparative analysis of CMOS pseudo differential amplifier and CMOS inverter based class AB pseudo differential amplifier using rail to rail CMFB circuit. In CMOS PDA complimentary CMFB circuit consisting of common mode detector, transimpedance and transconductance amplifier. But CMOS inverter based PDA circuit employs two CMOS inverters and CMFB consisting of current mode common mode detector and transimpedance amplifiers. The circuits have been designed using 0.18µm CMOS technology under 1 Volt supply and simulation results show that in CMOS inverter based PDA the rail to rail output swing is achieved with low common mode gain (-15dB).The output swing of circuit is 0.7V and power dissipation is 96Uw, which is less in comparison to 1V CMOS PDA.*

Keywords: *pseudo differential amplifier; common mode feedback; CMOS inverter*

1. INTRODUCTION

Nowadays, a high performance analog circuit using low voltage becomes essential mainly due to the advance of the large scale integration with complicated circuit systems and the demand for battery-operated portable equipments. However, supply voltage reduction in analog circuit causes several performance degradations and, therefore, new approaches in the design are needed to obtain analog circuits with enough bandwidth, gain and linearity. Operational transconductance amplifier (OTA) is one of the most basic cells as OTA finds many applications in many analog circuits such as operational amplifier, voltage comparators, A-D and D-A converters and high frequency filters. Several approaches have been proposed to design low voltage OTA [1-14] using both fully differential (FD) and pseudo-differential (PD) configurations. FD is typically based on a differential pair with a tail current source while PD is based on two independent inverters without tail current source. It is known that avoiding the voltage drop across the tail current source, in a PD structure, allows wider input and output ranges, and makes the architecture attractive for low power- supply applications. However, PD structure requires an extra common-mode feedback (CMFB) circuit, which serves two purposes: 1) to fix the common-mode voltage at high impedance nodes and 2) to suppress the common-mode signal components. Several approaches have been proposed to achieve CMFB [1-10]. Switched-capacitor circuit was proposed to build a CMFB [1], and the resulting circuit shows small power consumption. However, the CMFB circuits introduces clock-feed through error and load capacitance, [2-3] used simple resistive divider to sense the voltage of two differential nodes. As a result, the voltage swing of the CMFB is not limited. However, not only do these resistors require large silicon area, they load down the output impedances. [4] used MOS resistive network with bulk-driven CMFB technique. However, the circuit has quite low output impedance and high common gain. To solve the problem, methods of employing MOS transistor as CMFB circuit have been proposed [5-6]. The CMFB consists of CM detector and one stage amplifier. As a result, the common-mode gains are quite high and, in addition, the output swings are limited. [7-8] employs transistors with two stage common-mode amplifiers. The resulting common-mode gain is low. The problem with this structure is that the circuit has limited output swing and potential oscillation problem. [9-10] proposed the complementary CMFB, which can achieve both low common- mode gains with good output swings. However, the circuits are complex and show high power consumption. [11-12] proposed positive feedback technique to increase the differential gain. However, the circuit shows quite high common-mode gain (A_{cm} = -6 dB).

2. CIRCUIT DESCRIPTION

The circuit for CMOS pseudo differential amplifier is based on the configuration shown in Fig. 1. As seen, PDA consists of the input transconductor $G_{M(IN)}$ and common mode feedback network (CMFB). When the outputs from $G_{M(IN)}$ are differential signals, the currents through resistors R are of the same value but opposite phase. These currents will flow to each resistor and be mirrored to the Out1A and Out1B. Because these currents are of the same amplitude but opposite in phase, there will be no input current to the

transimpedance amplifier and no voltage variation at node C. The current through resistor R are also mirrored and positively feedback to the output of the input transconductor $G_{M(IN)}$. As a result, the output impedance of PD at node V_{o1} and V_{o2} are given by Z_{out}. When the outputs from PD are common mode signals, the common mode current will flow through nodes A and B with the same amplitude and phase. As a result, the summation of these two currents are added and passed to the common mode amplifier (A) which consists of transimpedance amplifier and output transconductor G_{MO}. The output current of G_{MO} is fed back to the output node of input transconductor $G_{M(IN)}$ to eliminate common mode signal. From Fig. 1, it can be easily shown that the common mode output impedance at the output nodes (V_{o1} and V_{o2}) are

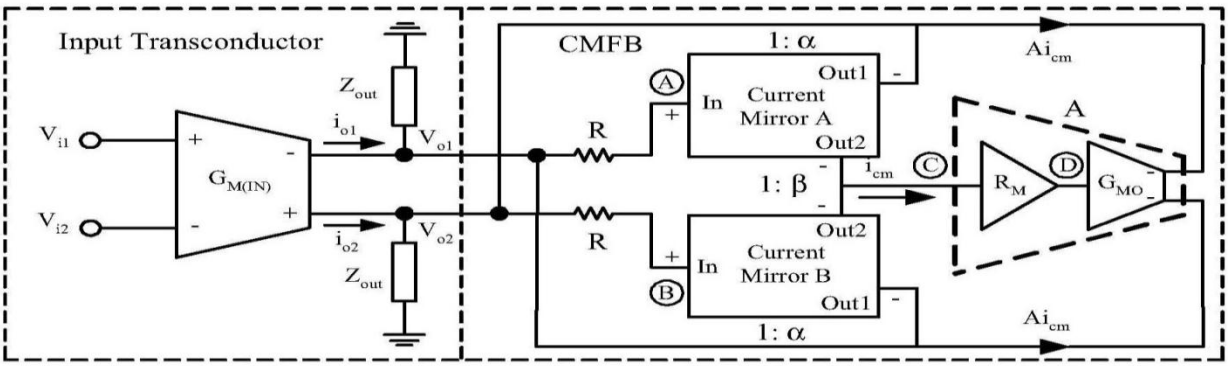

Fig. 1: Block Diagram of the proposed PDA

$$Z_{cm} = \frac{1}{g_{out} + (1+\alpha+2A\beta)/R} \quad (1)$$

Where the differential mode output impedance at the output nodes are

$$Z_{dm} = \frac{1}{g_{out} + (1-\alpha)/R} \quad (2)$$

where A,α,β and g_{out} are the gain of CMFB circuit. From equation 1 & 2 the common mode gain is

$$A_{cm} = G_{M(IN)}\left[\frac{1}{g_{out} + (1+\alpha+2A\beta)/R}\right] \quad (3)$$

similarly differential mode gain can be shown as

$$A_{dm} = G_{M(IN)}\left[\frac{1}{g_{out} + (1-\alpha)/R}\right] \quad (4)$$

From equation (3) and (4) the common mode rejection ratio is

$$CMRR = \frac{A_{dm}}{A_{cm}} = \left[\frac{g_{out} + (1+\alpha+2A\beta)/R}{g_{out} + (1-\alpha)/R}\right] \quad (5)$$

If A is large then CMRR can be increased.

Now, the description for a CMOS inverter based class AB pseudo Differential amplifier has been given below.

A. Conventional Class-AB OTA

A conventional class-AB OTA is shown in Fig. 1 (a). As seen, the circuit is based on CMOS inverter. It is well known that CMOS inverter has high gain and less power consumption. In addition, it contains no internal nodes and, as a result, the performance of the circuit will not be much degraded by the extra parasitic poles at high frequency. The PD structure using CMOS inverter is shown in Fig. 1 (b). It can be easily seen that the differential-mode gain (A_{dm}) is the same as the common-mode gain (A_{cm}), resulting in the unity common-mode rejection ratio ($CMRR=A_{dm}/A_{cm}$). Since large A_{cm} can lead to large common-mode variation at the output [13], therefore common-mode feedback (CMFB) circuit is required. Large A_{cm} can lead to large common-mode variation at the output [13], therefore common-mode feedback (CMFB) circuit is required.

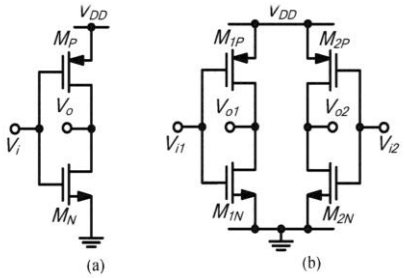

Fig. 1: (a) Inverter based single-ended OTA (b) Pseudo-differential OTA

B. The Proposed PDA Structure

The proposed PDA is based on the configuration shown in Fig. 2(a). As seen, PDA consists of the two independent CMOS inverters ($M_{1N,p}$ - $M_{2N,p}$) and common-mode amplifier (CMA), which serves two purposes: 1) to detect the common- mode signal at the output nodes (V_{o1} and V_{o2}), and 2) to provide positive feedback (see dash line) to enhance the output impedance and differential gain.

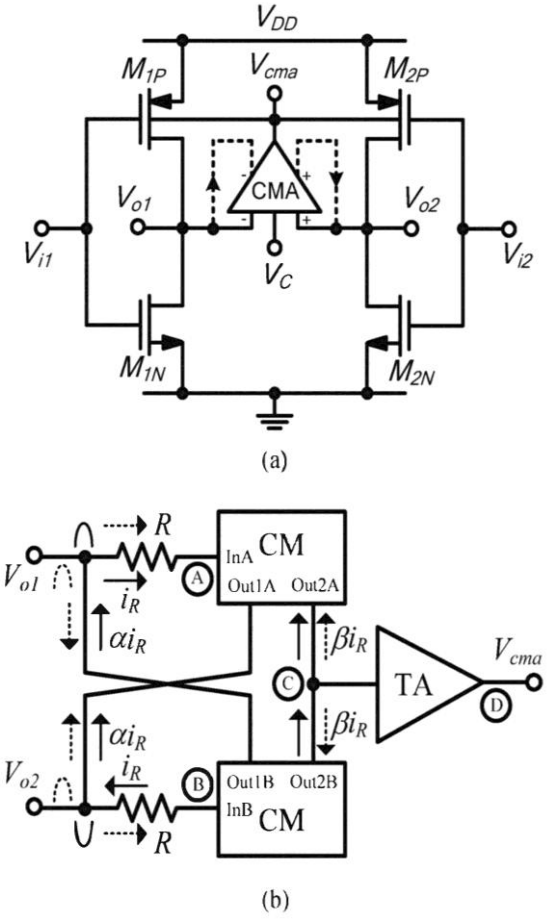

Fig. 2: The proposed PDA (a) Circuit configuration (b) Structure of CMA

The operation can be explained as follows. In case of the common-mode output signal ($V_{o1,2}$= V_{oc}), CMA will amplify $V_{o1,2}$ and negatively fed back the result (V_{cma}) to the bulk terminals of $M_{1P,2P}$ such that the common-mode output voltage is suppressed. On the contrary, CMA will not respond to the differential-mode signal (V_{o1}= - V_{o2}), namely, the output of CMA (V_{cma}) stays constant. The DC common-mode voltage is set by V_c. It is noted that the common-mode gain can be further suppressed if V_{cma} is also fed back to the bulk terminals of $M_{1N,2N}$ This can be made possible in the triple-well process. Fig. 2(b) illustrates the architecture of the proposed CMA. As seen, CMA consists of two matched resistors (R), two current mirrors (CM) and transimpedance amplifier (TA). The operation of the CMA can be explained as follows. When the output voltages from PDA are differential signals (see solid signal), these voltages are converted to the currents through resistors R. These currents, which have the same magnitude but opposite phase, flow to each resistor and are mirrored to the Out_{2A} and Out_{2B} terminals (with the current gain of β). Because these currents have the same magnitude but opposite phase, there will be no input current flowing into the transimpedance amplifier (TA) and, thus no voltage variation at node C. In addition, the currents through resistors R are mirrored to the Out_{1A} and Out_{1B} terminals (with the current gain of α), and positively fed back to the output of the PDA, thus enhancing the output impedance (at nodes V_{o1} and V_{o2}) and differential gain of the system. When the outputs from PDA are common-mode signals (see dotted line), the common-mode current flows through nodes A and B with the same amplitude and phase. As a result, the summation of these two currents are added constructively and passed to transimpedance amplifier (TA). The amplified output voltage V_{cma} is negatively fed back to the bulk terminals of $M_{1P,2P}$ to suppress the common-mode voltage, as discussed previously. Straight forward small signal analysis shows that A_{dm} and A_{cm} can be derived and shown as

$$A_{dm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+(1-\alpha)Z_{out}/R}\right] \quad (1)$$

$$A_{cm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+\left(1+\alpha-2g_{mb}\beta R_F\right)Z_{out}/R}\right] \quad (2)$$

Where $G_{M(IN)}$ is the transconductance of the CMOS inverter ($G_{M(IN)}$ =$gm_{1N,2N}$ + $gm_{lp,2P}$), Z_{OUT} is the output impedance of the PDA (Zout=$r_{O1N,2N}$/$r_{O1P,2P}$), α and β are the current gains of the current mirror (CM), g_{mb} is the bulk transconductance of $M_{1P,2P}$, and R_F is the transimpedance gain of the transimpedance amplifier.

From eq (1) & (2), one can find the common mode rejection ratio as

$$CMRR = \frac{A_{dm}}{A_{cm}} = \left[\frac{1+\left(1+\alpha-2g_{mb}\beta R_F\right)Z_{out}/R}{1+(1-\alpha)Z_{out}/R}\right] \quad (3)$$

From Eq. (3), one can notice that CMRR can be increased if the transimpedance gain (R_F) is large. In addition, the current gain α and β of current mirrors A and B also play roles in determining the CMRR.

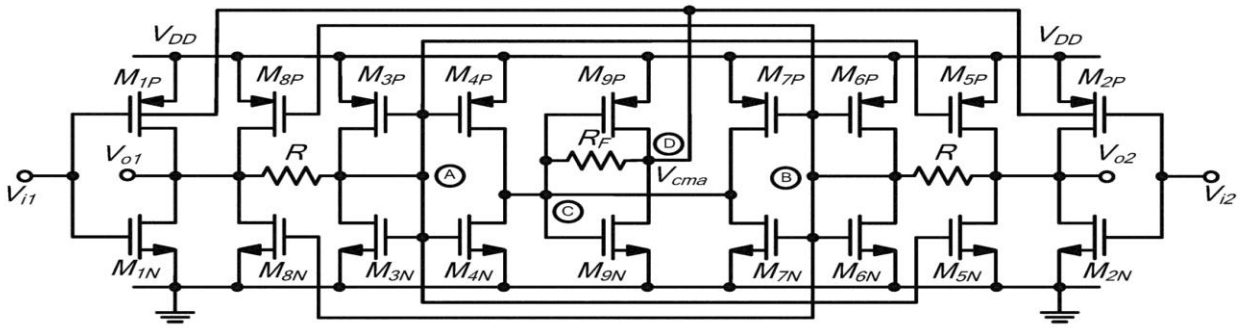

Fig. 3: The proposed class AB pseudo-differential amplifier (PDA)

3. CIRCUIT IMPLEMENTATION

The circuit implementation of Fig.1 for CMOS pseudo differential amplifier is given as in [15].

The circuit implementation of Fig. 2 is illustrated in Fig. 3. $M_{lN,P}$-$M_{2N,P}$ consist to be the input pseudo-differential amplifier, while $M_{3N,P}$-$M_{9N,P}$ consist to be a wide swing CMFB circuit. $M_{3N,P}$-$M_{5N,P}$ form the current mirror A while $M_{6N,P}$- $M_{8N,P}$ are used to form the current mirror B. The current gain with the ratios of α and β can be achieved by adjusting the aspect ratios of $M_{3N,P}$, $M_{5N,P}$ ($M_{6N,P}$, $M_{8N,P}$) and $M_{3N,P}$, $M_{4N,P}$ ($M_{6N,P}$, $M_{7N,P}$), respectively.

It is noted that the choice of α requires precaution. A large value of α can result in a large differential gain. However, large value of α can drive the circuit unstable. In practice, α should be set a little bit larger than one to compensate for the loss, due to the imperfection of the current mirror not being able to perfectly mirror the current from the input to the output. In this work, α is set to 1.3 to enjoy both differential gain and stability. The value of β plays role in determining the common-mode gain, because it is part of the CMFB circuit. As seen in Eq. (2), large value of β results in low common- mode gain. However, it is noted that large β requires large transistors, thus large standby current and parasitic capacitors, which can degrade frequency performance of the system. In this work, β is set to 3.

Transistor $M_{9N,P}$ and R_F consist to be the transimpedance amplifier (TA). The transimpedance gain of the circuit is set by the resistor R_F. The transimpedance amplifier is employed here to enhance the gain of the common-mode amplifier (CMA) and, at the same time, to reduce both input and output impedances (at nodes C and D), so that the time constants associated with these nodes are low. The dc common-mode voltage level (V_c) is equal to the voltages at nodes A and B, which is given by [14]

$$V_C = \frac{V_{DD} - V_{TN(3N,6N)} + V_{TP(3P,6P)}}{1+\sqrt{\beta_{N(3N,6N)}/\beta_{P(3P,6P)}}} + V_{TN(3N,6N)} \qquad (4)$$

where $\beta_{N(3N,6N)}=\mu_n C_{Ox}(W/L)_{3N,6N}$ and $\beta_{p(3p,6p)}=\mu_p C_{ox}(W/L)_{3P,6P}$

For maximum output swing, we have set $\beta_{N(3N.6N)}$ and $\beta_{p(3P,6p)}$ such that V_c is equal to $V_{DD}/2$.

4. SIMULATION RESULTS

To verify the circuit performance, HSPICE is used to simulate the proposed circuit, using a 0.18 µm. CMOS process under the supply voltage of 1 V. In this work, the bias currents of all transistors are chosen to optimize both gain and power dissipation. CMOS pseudo differential amplifier and CMOS inverter based class-AB pseudo differential amplifier show following characteristics.

A. DC transfer characteristic:

Fig. 4(a) and Fig.4(b) show the DC transfer characteristic for CMOS PDA and CMOS inverter based PDA respectively. In both type of PDAs output swing shows rail to rail operation.

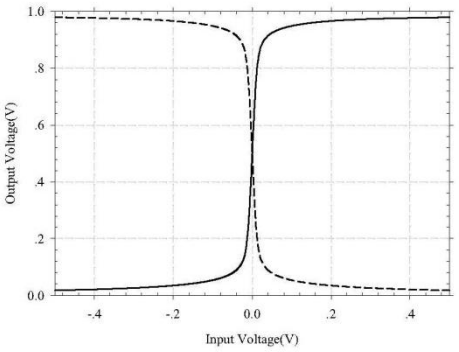

Fig. 4(a): DC transfer characteristics

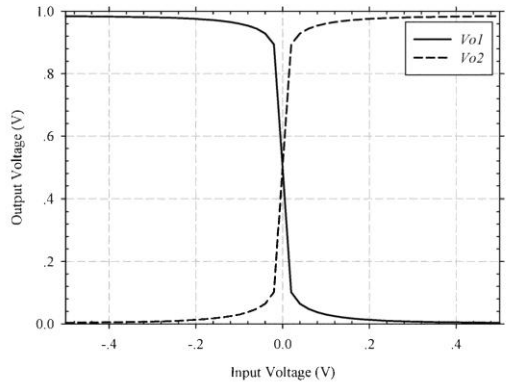

Fig. 4(b): DC transfer characteristics

B. Transient response of output voltage:

Fig.5(a) and Fig.5(b) show differential & common mode voltages. As seen in CMOS PDA differential voltage is ±0.7V & variation in common mode voltage is 0.3mV.But in CMOS inverter based PDA differential and common mode output voltages are 0.7Vp-p & 0.4mVp-p.

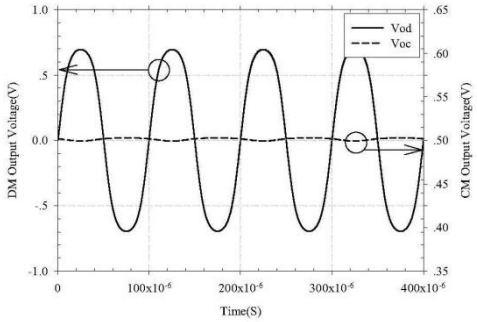

Fig. 5(a): Differential & common mode output voltages

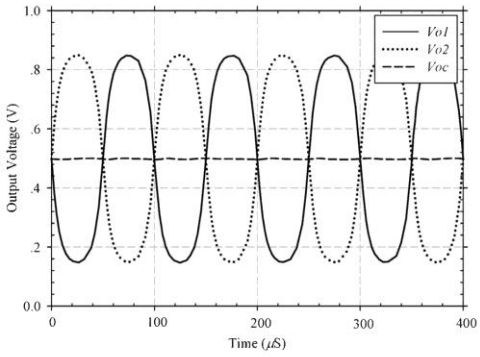

Fig. 5(b): Differential & common mode output voltages

C. Frequency response for DM input signal:

Fig. 6 shows the frequency response in case if differential mode input signal. In Fig.6(a) DC gain is found to be 36dB,while -3dB and unity gain frequency are 14MHZ and 1.25GHZ respectively while phase margin is 87°. As seen in Fig. 6(b) the DC gain is found to be 36 dB, while the -3 dB and unity gain frequency are 8.5 MHz and 800 MHz, respectively. The phase margin is 85°.

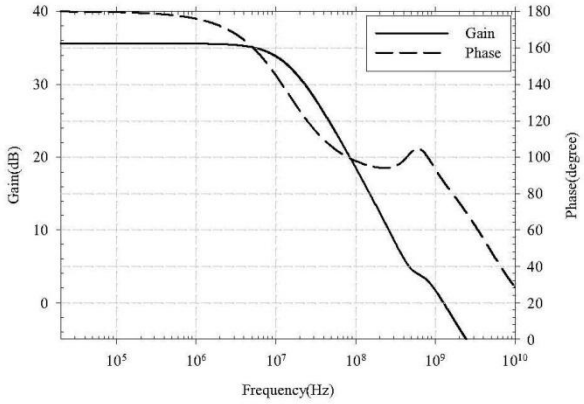

Fig. 6(a): Gain and phase margin of DM

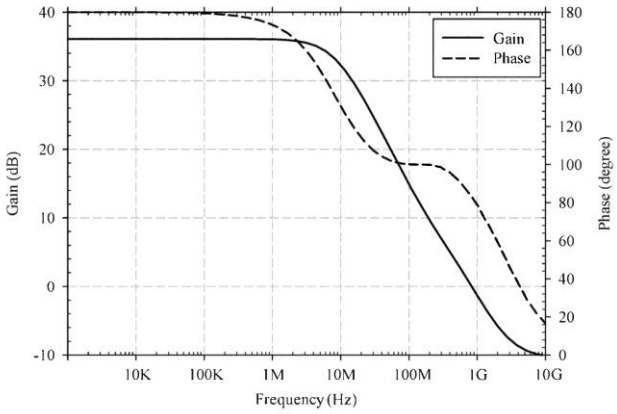

Fig. 6(b): Gain and phase margin of DM

D. Frequency response for CM input signal:

Fig. 7 shows the frequency response of the PDA in case of the common-mode input signal. As seen in Fig. 7(a) common mode gain is -36dB and power dissipation is 0.23mW but Fig. 7(b) shows the common-mode gain is relatively much smaller (-15 dB), while the bandwidth is almost the same as in the differential-mode case. The power dissipation of CMOS inverter based class-AB pseudo differential amplifier is 96 µW.

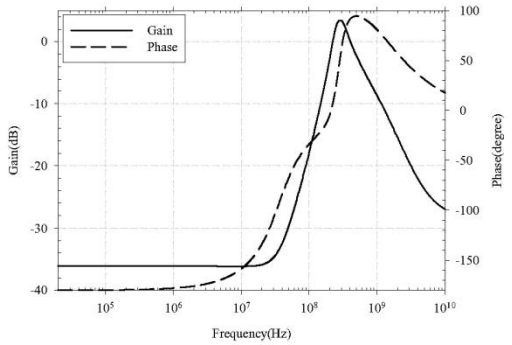

Fig. 7(a): Gain and phase margin of CM

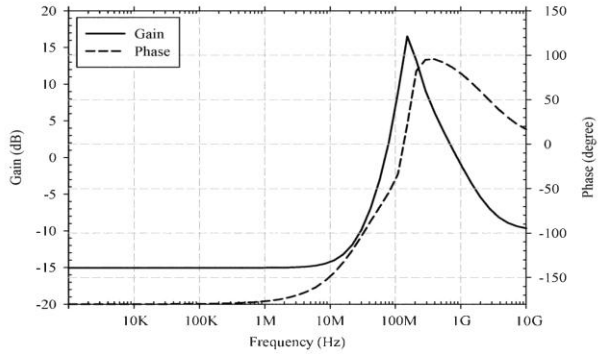

Fig. 7(b): Gain and phase margin of CM

5. CONCLUSION

In this paper a CMOS PDA and CMOS inverter based PDA are used, which operate on low voltage and use CMFB circuit. Simulation results show that in CMOS inverter based PDA common mode gain is -15dB, unity gain frequency is 800MHZ, phase margin is 85^{o} and power dissipation is 96µW which is very small in comparison to 1 volt CMOS pseudo differential amplifier.

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